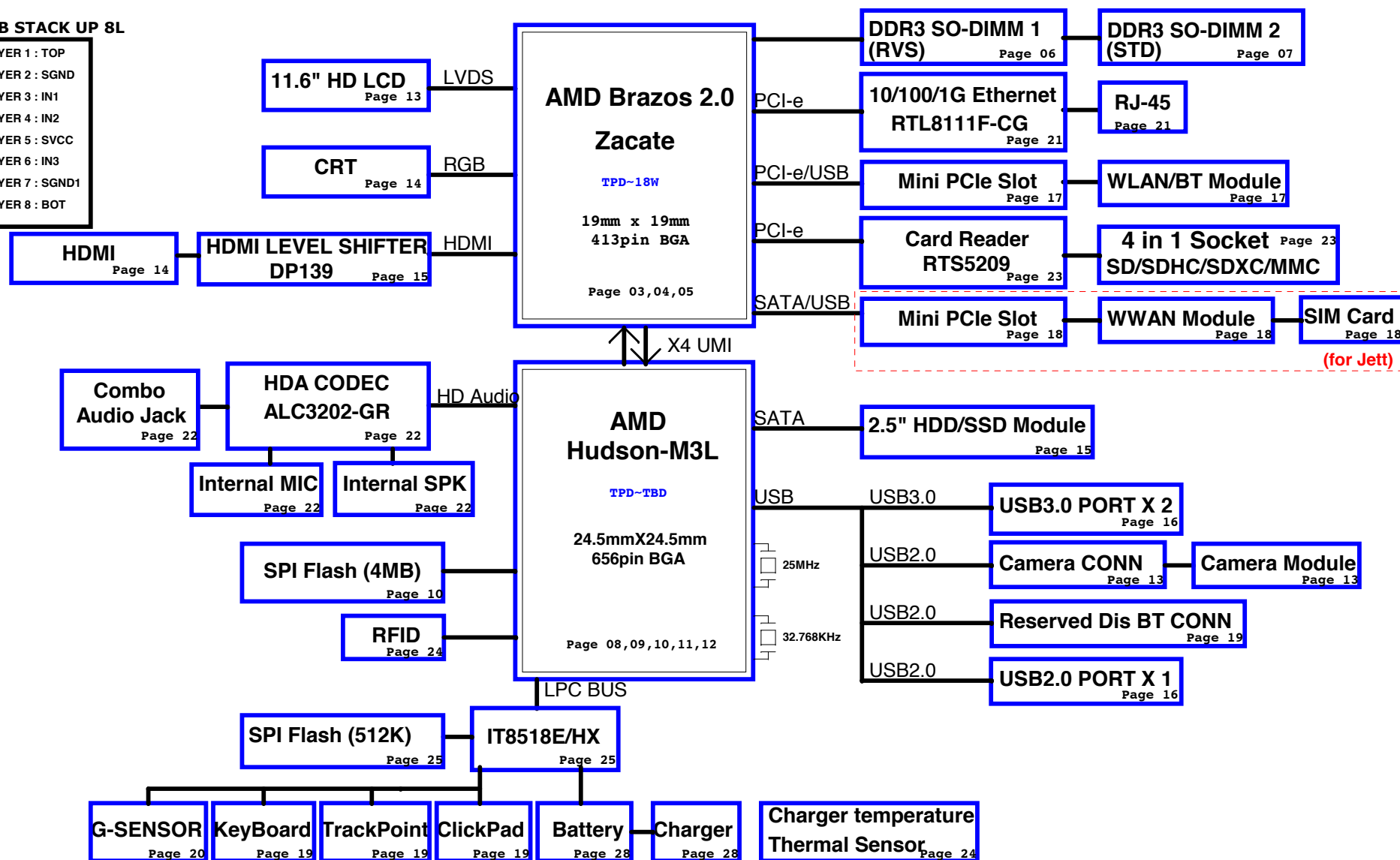


# Dutton & Jett Note Block Diagram -- AMD Brazos 2.0

## PCB STACK UP 8L

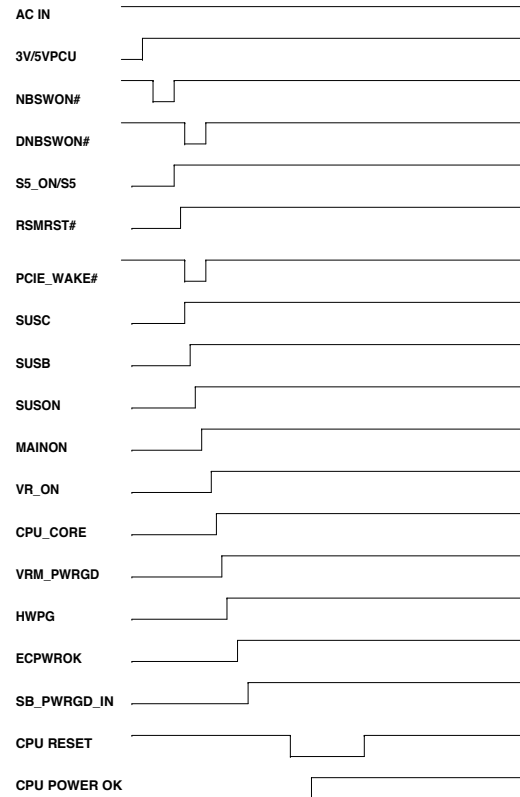
LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : IN3  
LAYER 7 : SGND1  
LAYER 8 : BOT



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2	SYSTEM INFORMATION	
3	Zacate MEM & PCIE I/F(1/3)	
4	Zacate DISPLAY/CLK/MI(2/3)	
5	Zacate POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM RVS (H=4.0)	
7	DDR3 SO-DIMM STD (H=4.0)	
8	FCH M3L GPIO/USB/AZ(1/5)	
9	FCH M3L PCIE/CLK/LPC(2/5)	
10	FCH M3L SATA/HWM/SP(3/5)	
11	FCH M3L POWER/GND(4/5)	
12	FCH M3L Strap(5/5)	
13	CONN LCD/CAMERA	
14	CONN CRT/HDMI CONN	
15	CONN SATA(HDD or SSD)	
16	CONN USB3.0x2+USB2.0x1	
17	CONN WLAN+BT Combo	
18	CONN WWAN or mSATA	
19	CONN KB/TP	
20	CONN BT/G-SENSOR	
21	LAN_RTL8111F-CG	
22	AUDIO_ALC3202-VC3-GR	
23	Card Reader_RTS5209-GR	
24	FAN/Thermal/LED/RFID	
25	KBC IT8518E/HX	
26	Screw Hole/EM/ESD	
27	POWER_Power Diagram	
28	POWER_CHARGER (BQ24707)	
29	POWER_5V/3V (TPS51123)	
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36	Schematic Value Descript	
37	EC RECORD Before A stage	
38	EC RECORD After A stage	
39	EC RECORD After B stage	
40	EC RECORD After C stage	

## Power Sequence

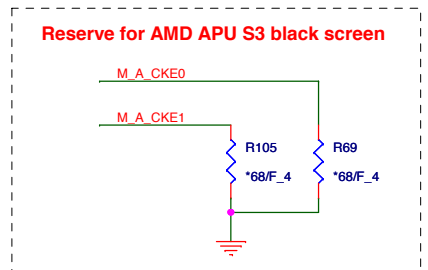


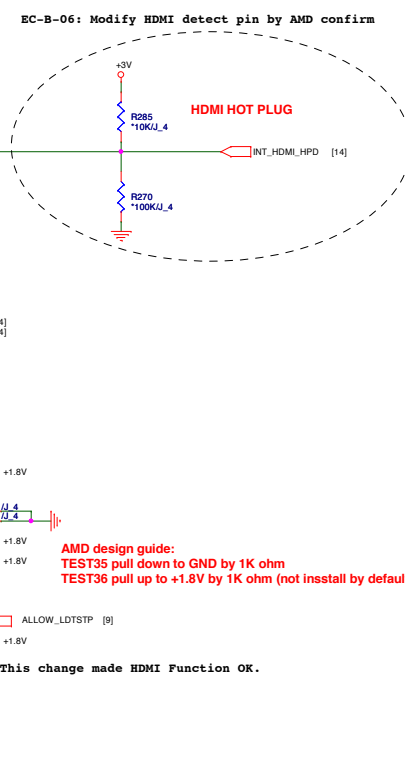
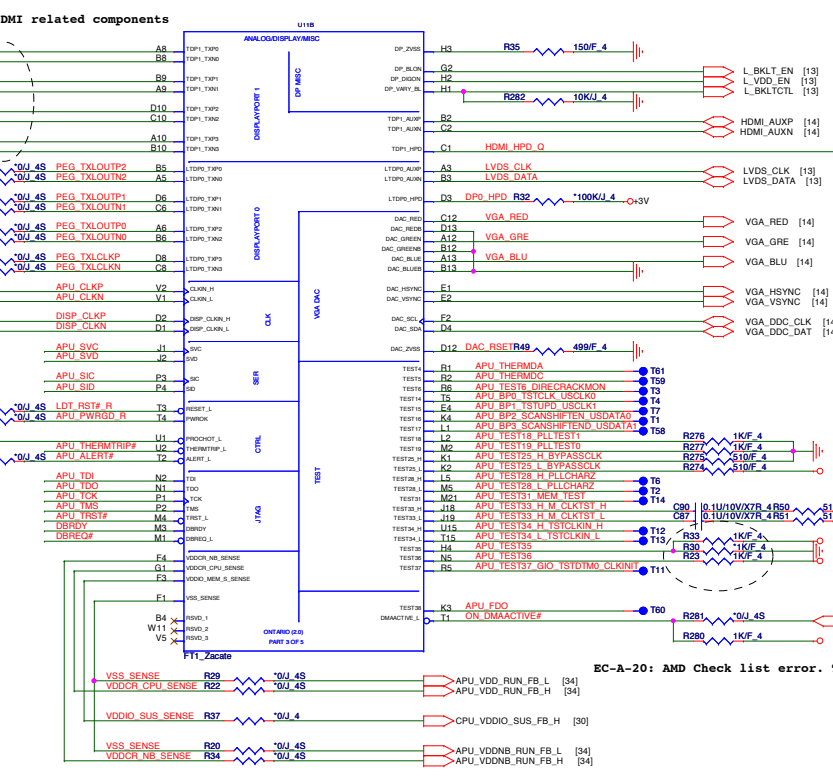
## Hudson M3L SM BUS

M3L SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (Pull Up By "+3V")	AD26 AD25	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (Pull Up By "3V_S5")	T7 R7	not used
SB_SCLK2 SB_SDATA2 (Pull Up By "3V_S5")	H19 G19	not used
SB_SCLK3 SB_SDATA3 (Pull Up By "3V_S5")	G22 G21	not used
SB_SCLK4 SB_SDATA4	J19 K19	not used

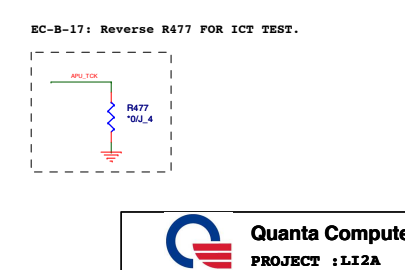
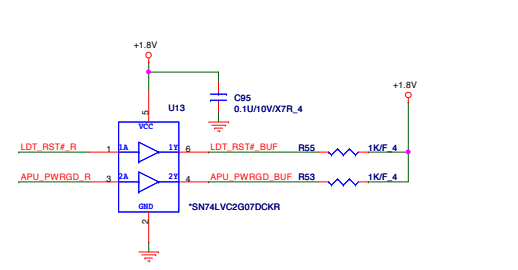
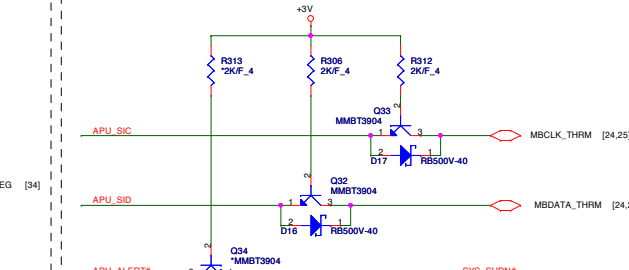
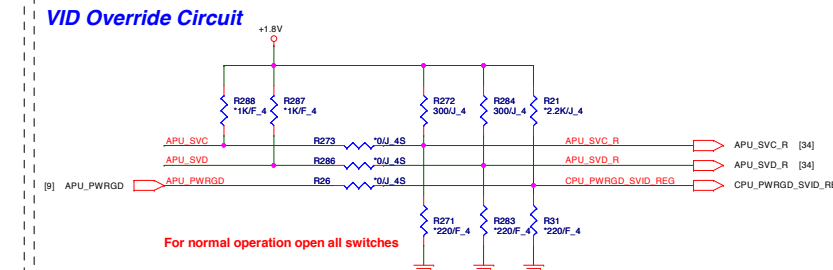
## KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (Pull Up By "3V_PCU")	110 111	Battery
MBCLK_THRM MBDATA_THRM (Pull Up By "3V_PCU")	115 116	Thermal

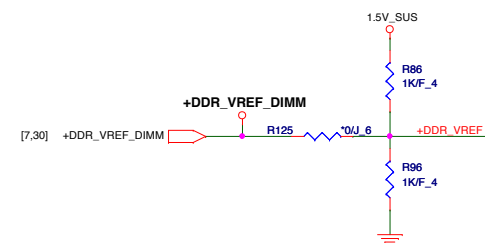
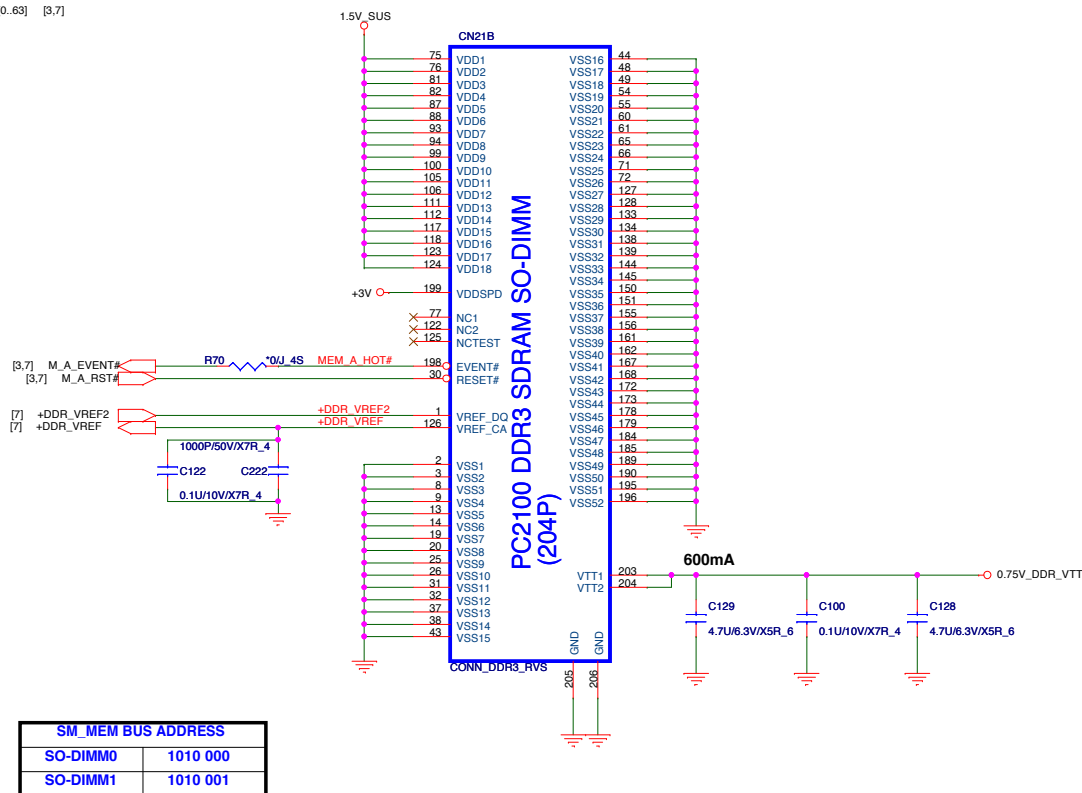


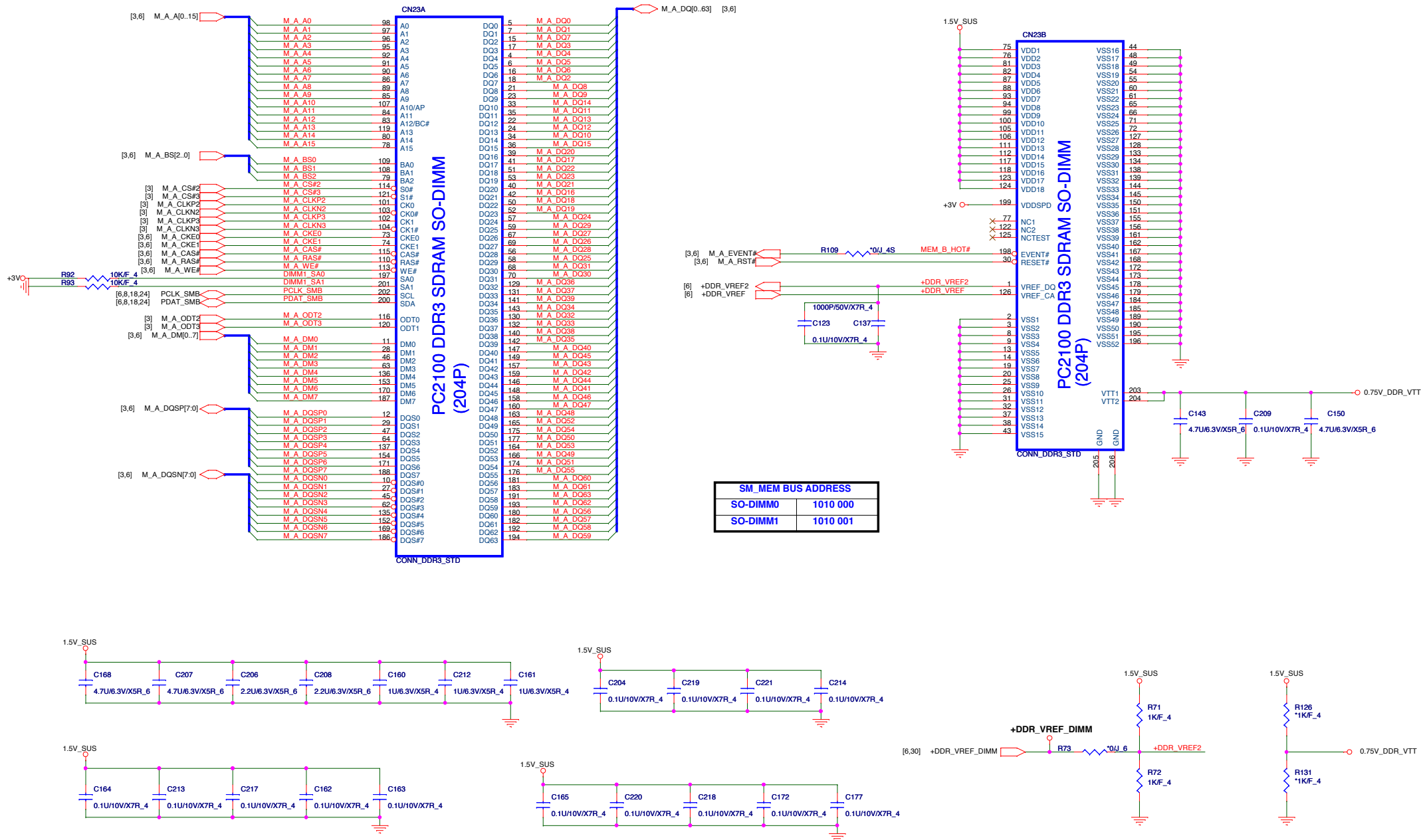


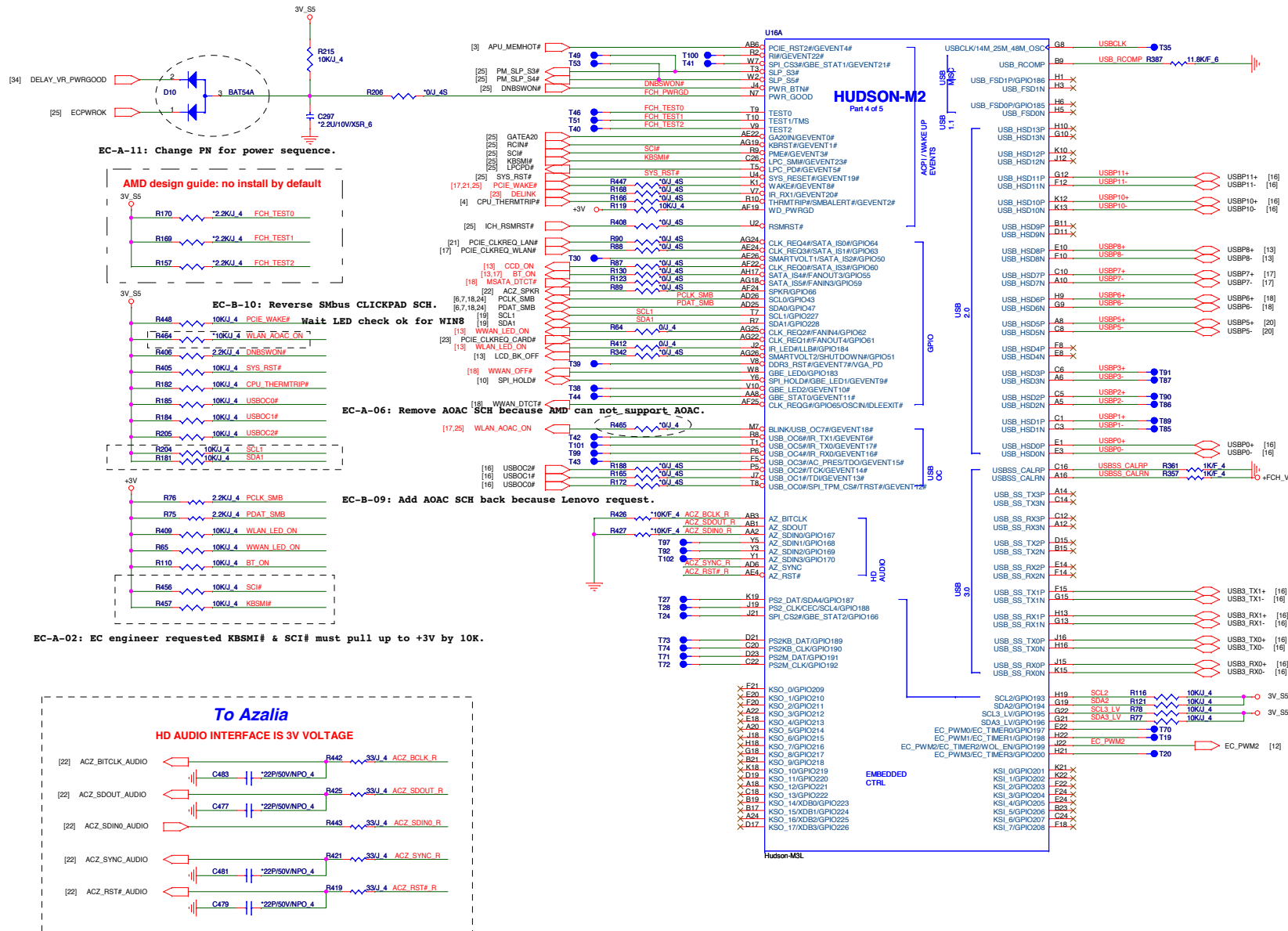
EC-A-20: AMD Check list error. This change made HDMI Function 0

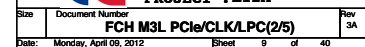


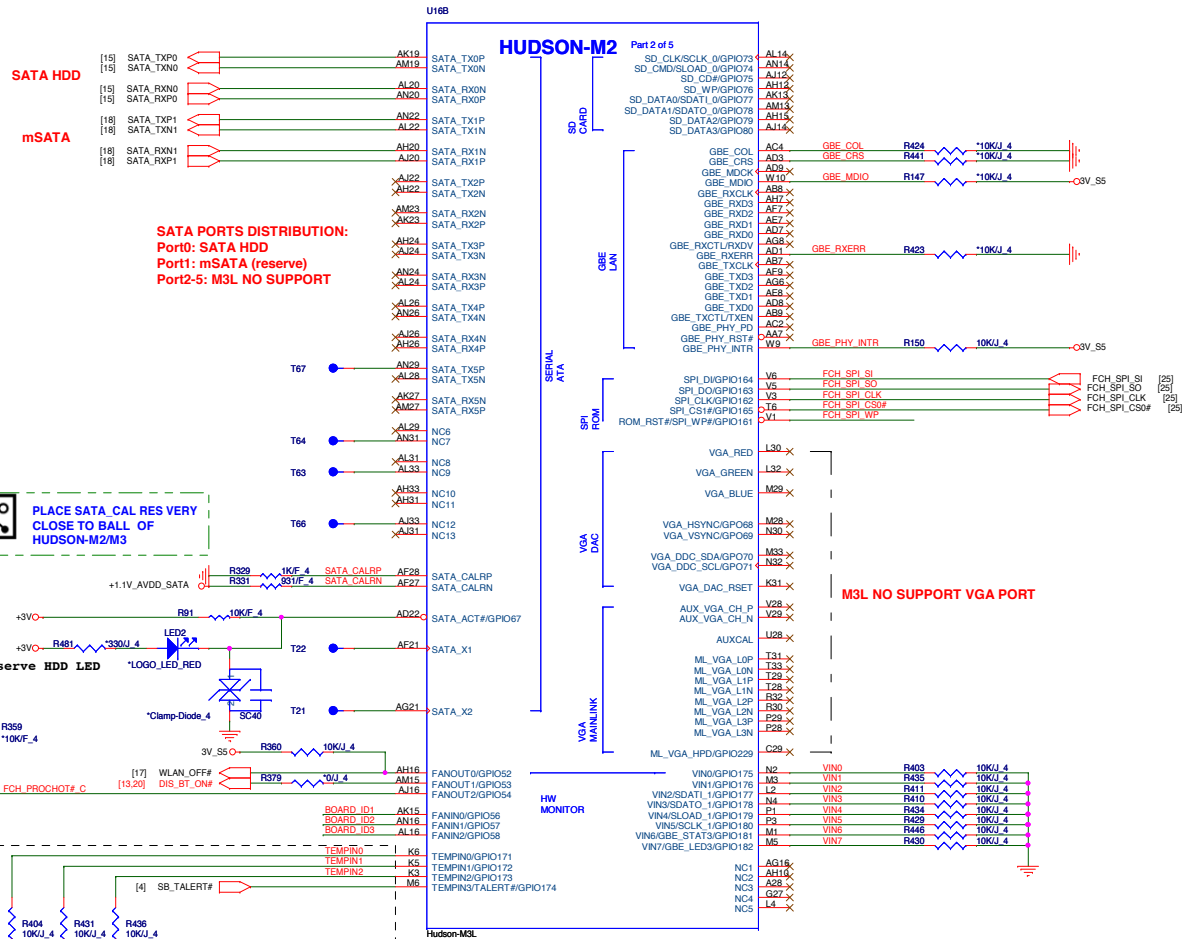




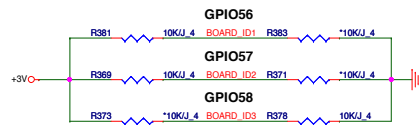








### BOARD ID SETTING (default low)

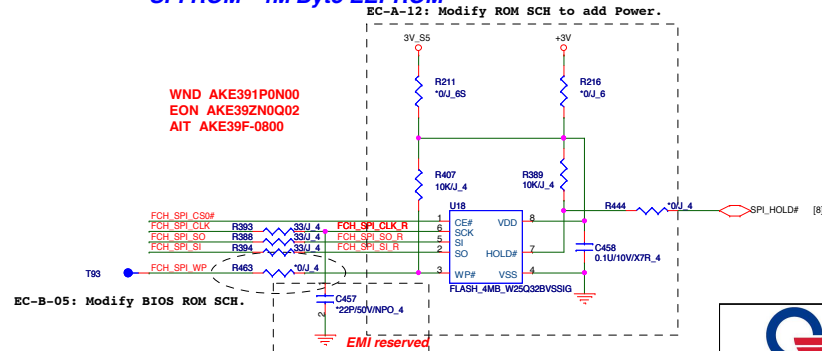


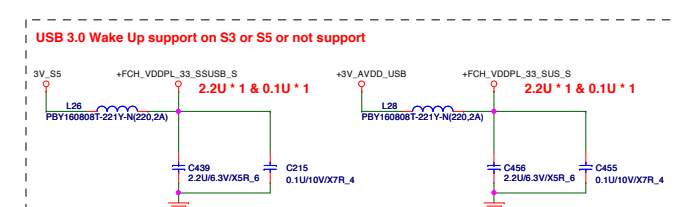
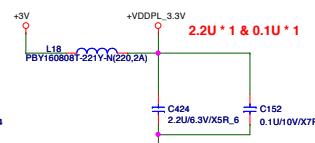
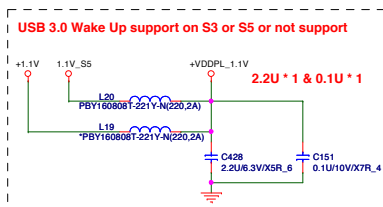
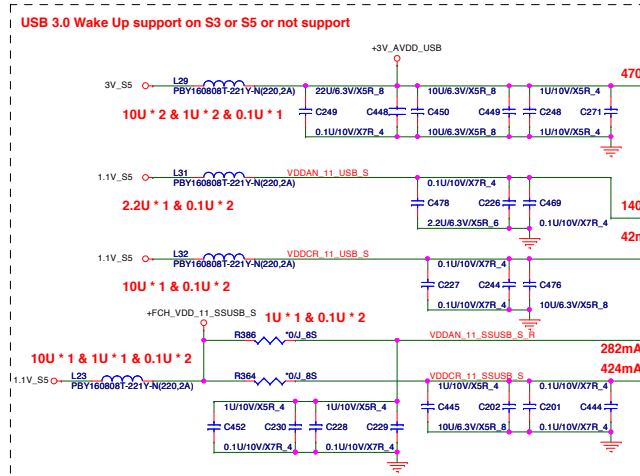
GPIO56: HIGH/LOW ==> JETT/DUTTON

GPIO57: HIGH/LOW ==> E2-1800/E1-1200

	GPIO57	GPIO56
HIGH	31LI2MB00F0	31LI2MB00G0
LOW	31LI2MB00H0	31LI2MB00I0

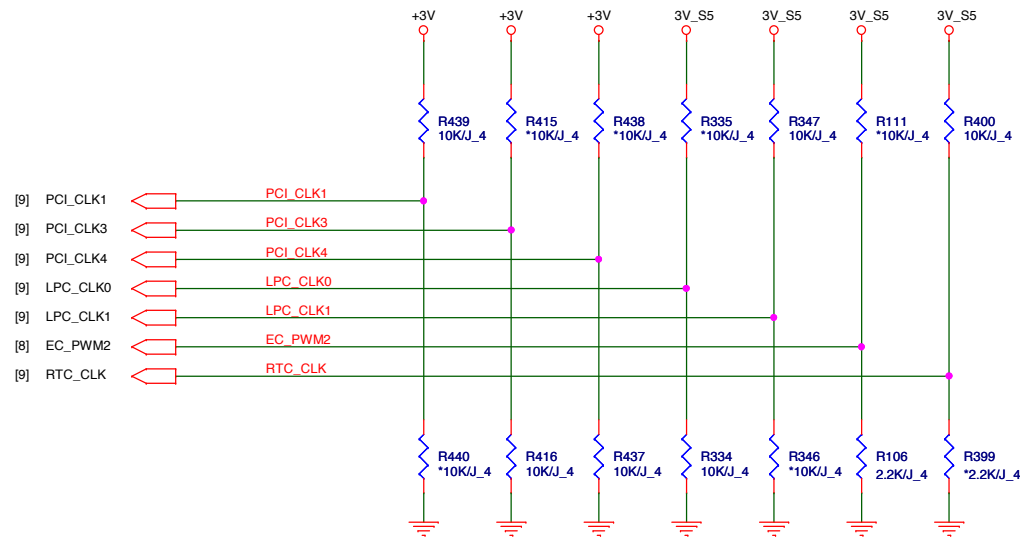
### SPI ROM - 4M Byte EEPROM







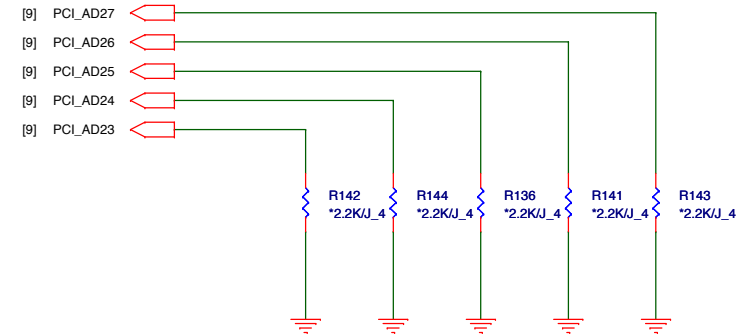
OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.



#### REQUIRED STRAPS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE Gen2 DEFAULT	USE DEBUG STRAP	NON_Fusion CLOCK MODE	INT EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE Gen1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	INT EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]



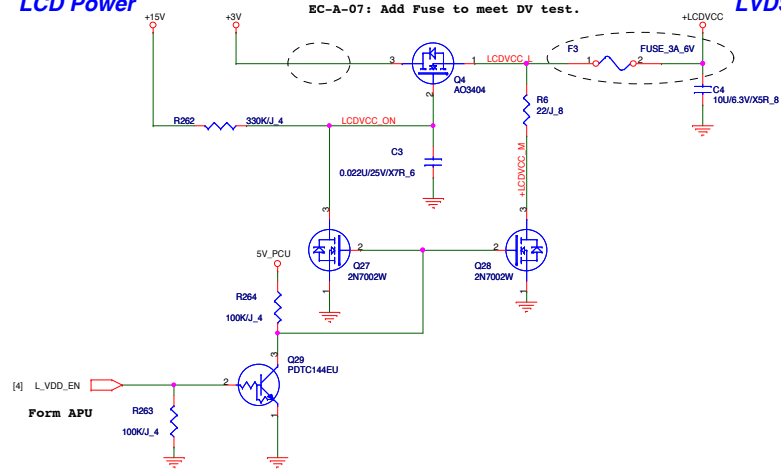
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



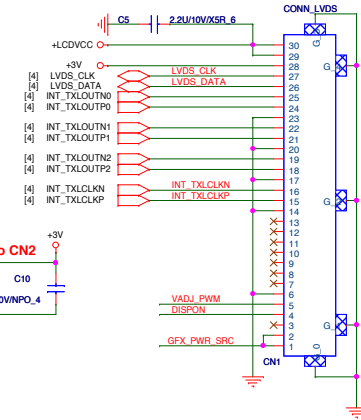
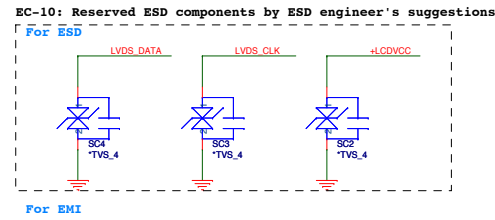
Quanta Computer Inc.  
PROJECT : LI2A

Size	Document Number	Rev
	FCH M3L Strap(5/5)	3A
Date:	Monday, April 09, 2012	Sheet 12 of 40

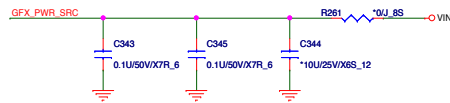
### LCD Power



**LVDS (11.6" HD) CONN**

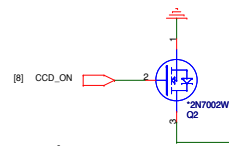


**CCD+LOGO+WLAN LED CONN**



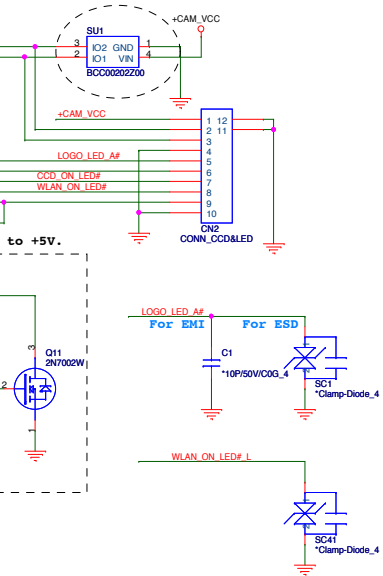
EC-A-22: EE request in order LED action error by DIS\_BT

EC-C-01: Drop CCD Led relation BOM.

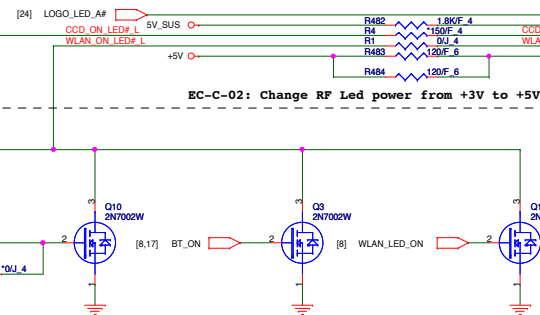


EC-C-10: Remove CML1 & R5 & R8 in order to place R483 & R484

EC-A-21: ESD request.



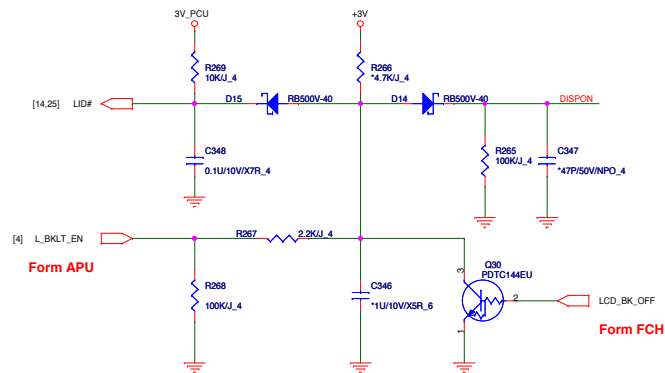
EC-A-19: Lenovo modify LED brightness.



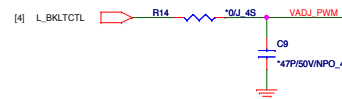
**EC-C-02: Change RF Led power from +3V to +5V.**

EC-23: add WWAN, WLAN, BT LED SCH to match Jett spec

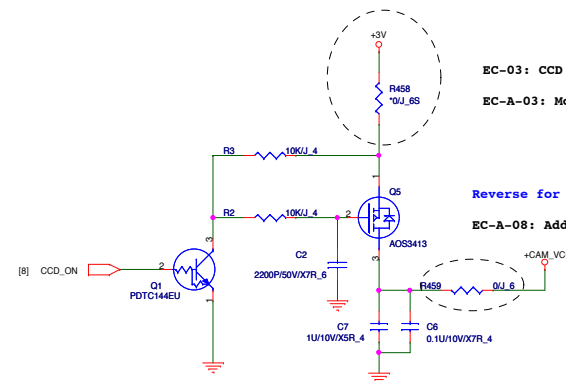
### *Back Light*



**PWM**



### ***CAMERA VCC Control***

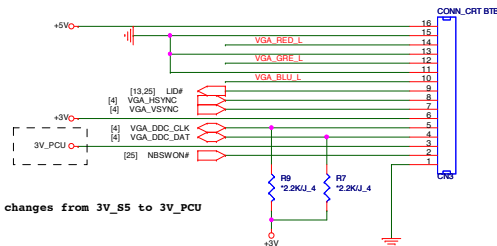


**EC-03: CCD power changes from +5V to +3V**

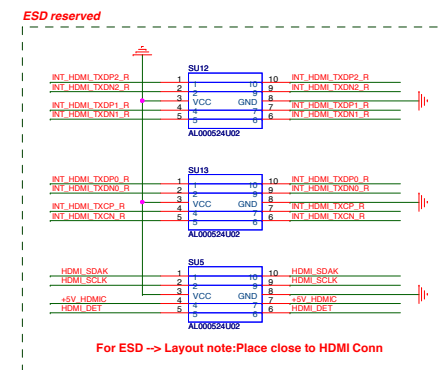
EC-A-03: Modify CCD power source width.

Reverse for FUSE function.

EC-A-08: Add 0 ohm to CCD power.



EC-19: Hall IC power changes from 3V\_S5 to 3V\_PCU



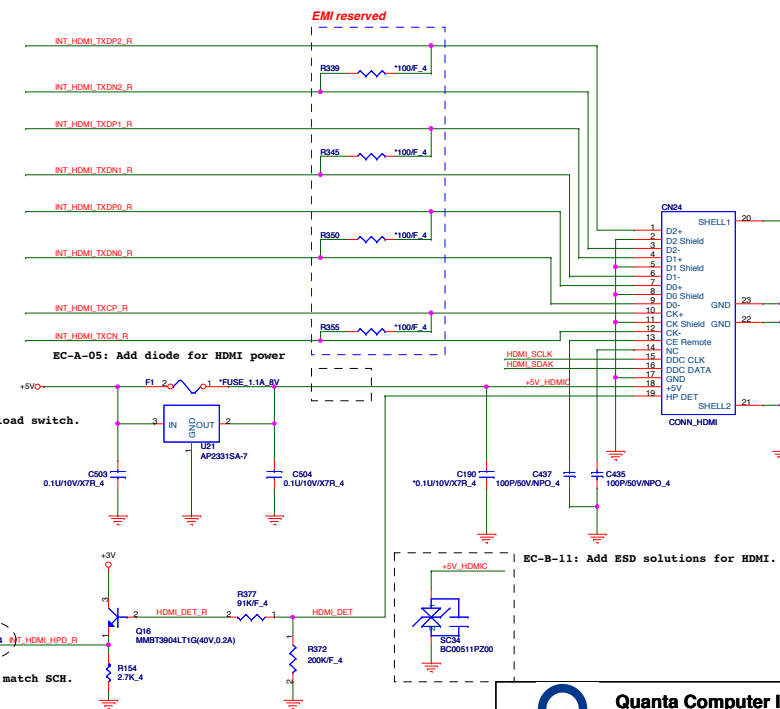
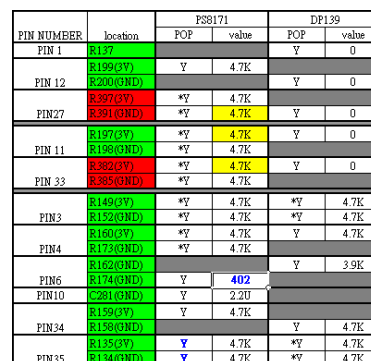
For ESD --> Layout note: Place close to HDMI Conn


## HDMI CONN



EC-02: Remove AMD HDMI related components

### HDMI Level Shifter

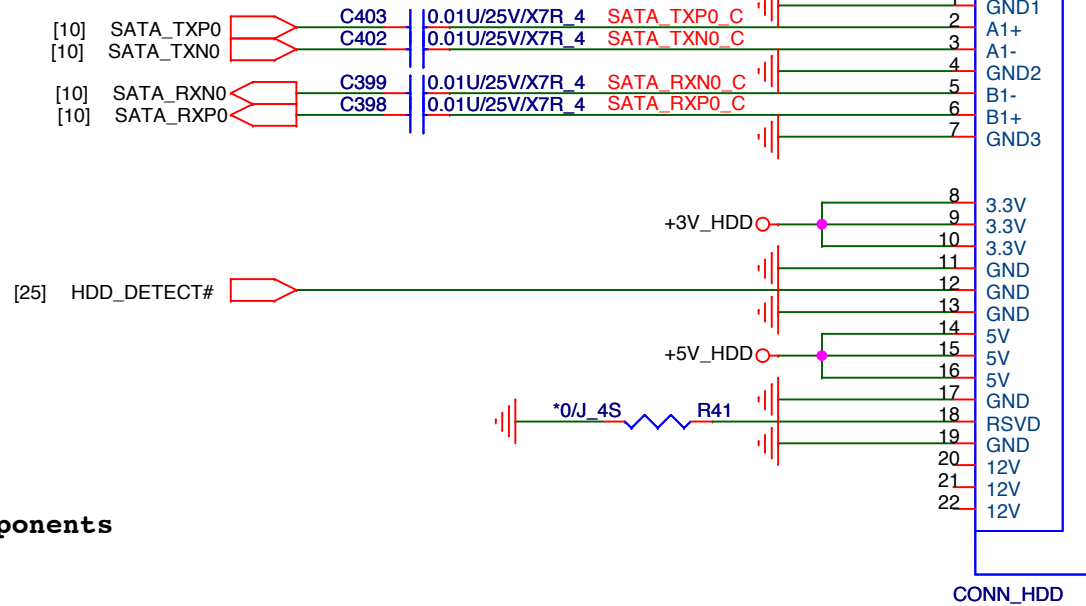



**Quanta Computer Inc**  
**PROJECT : LI2A**  
 Size Document Number  
**CONN CRT/HDMI CONN**  
 Date: Monday, April 06, 2015 8:48:14 AM

# SATA HDD CONN

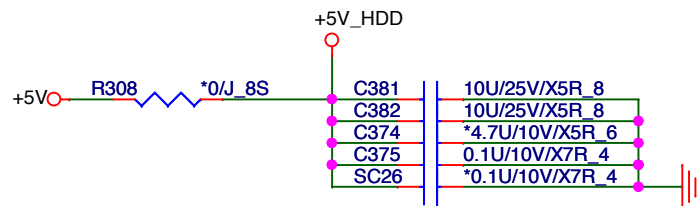
15

## From FCH SATA



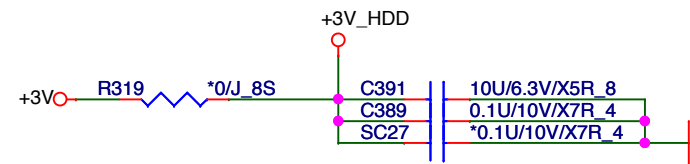
EC-01: Remove SATA redriver & other components

DC Current rating: 2 A (MAX)



EC-16: Reserved ESD components  
by ESD engineer's suggestions

DC Current rating: 3 A (MAX)

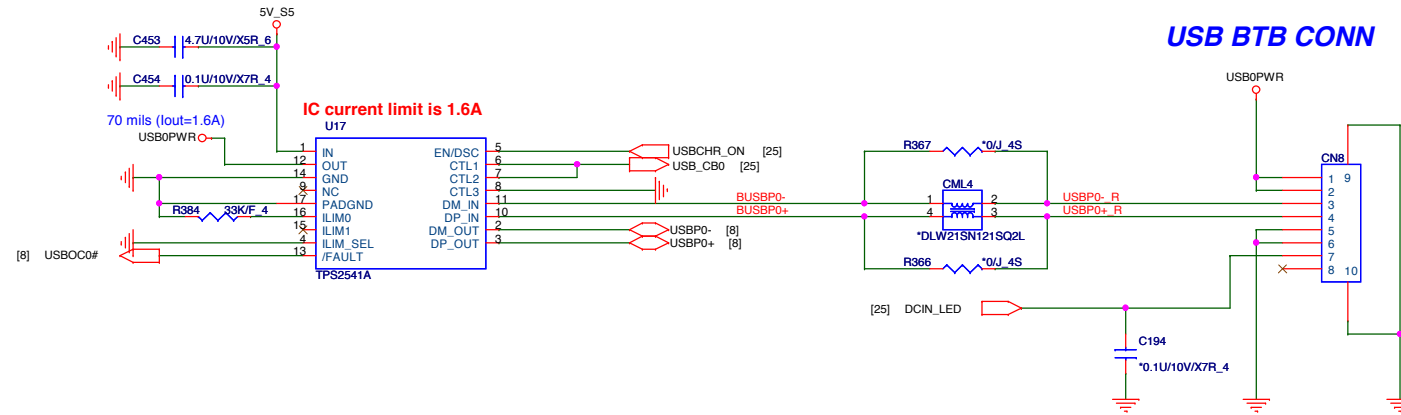


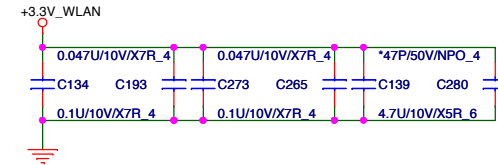
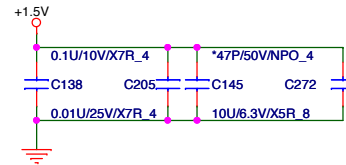
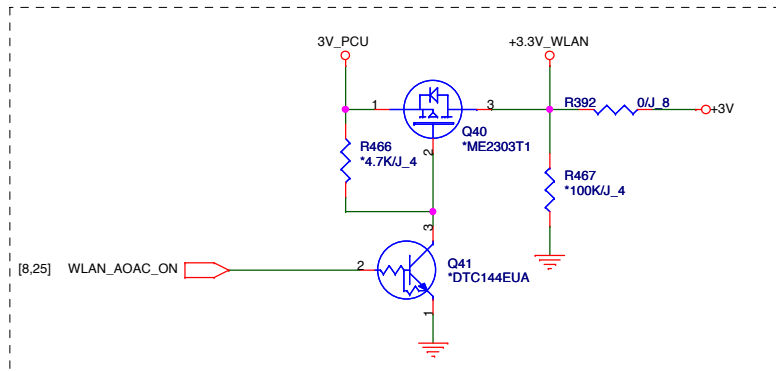
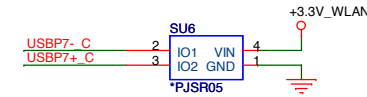
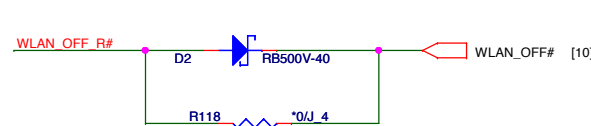
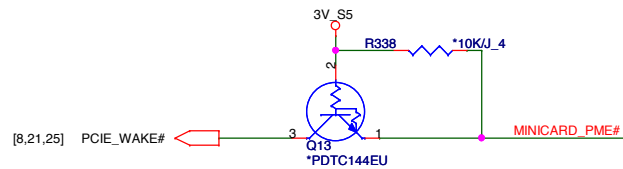
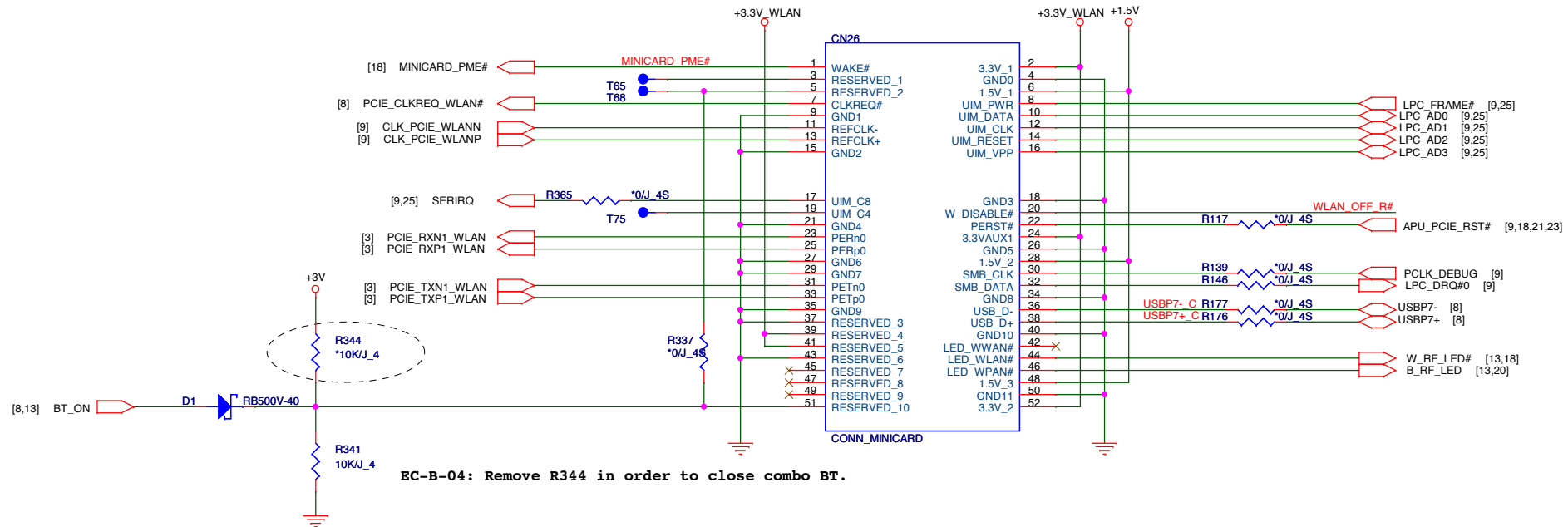
Quanta Computer Inc.

PROJECT : LI2A

Size	Document Number	Rev
	CONN SATA(HDD or SSD)	3A
Date:	Monday, April 09, 2012	Sheet 15 of 40

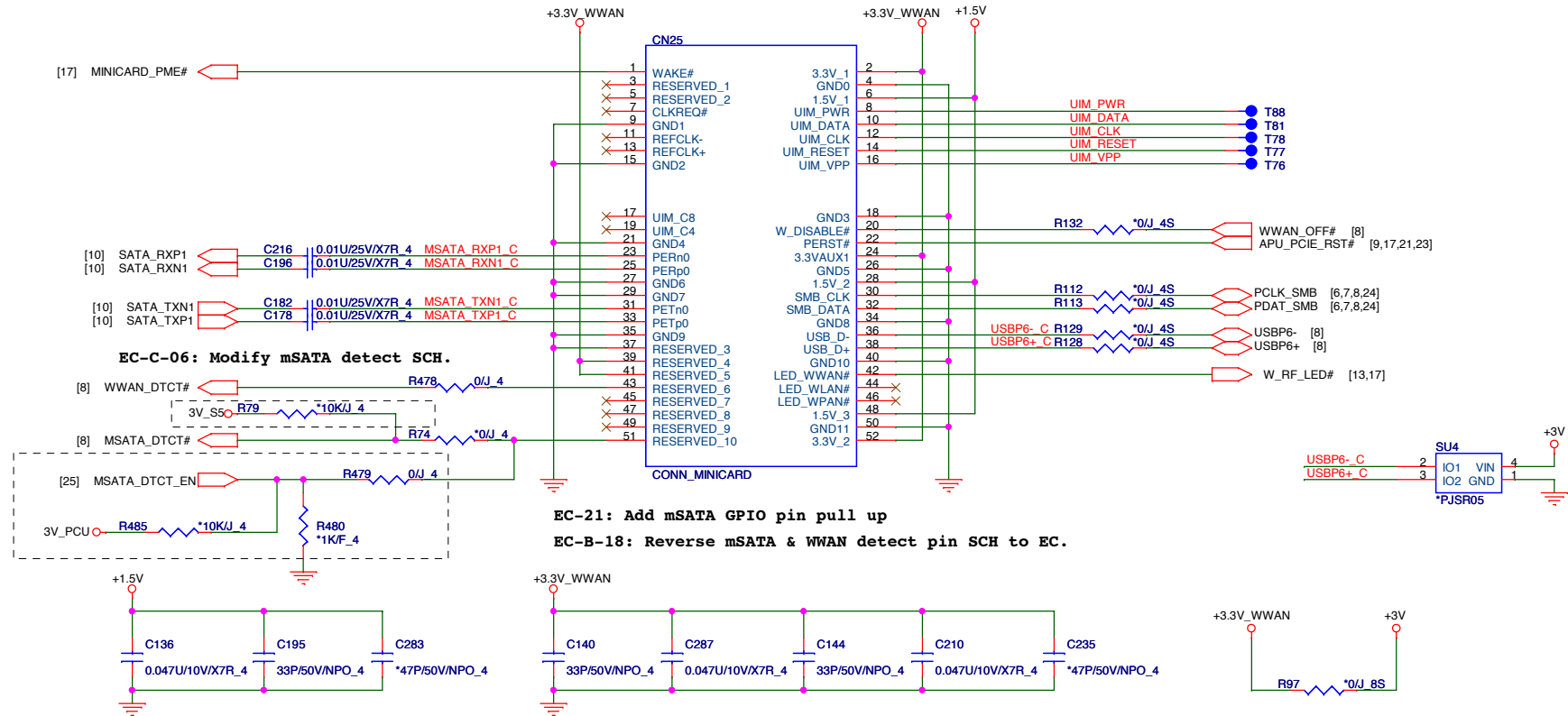
## USB2.0 Port0



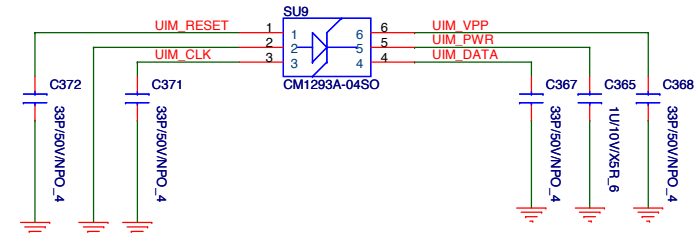
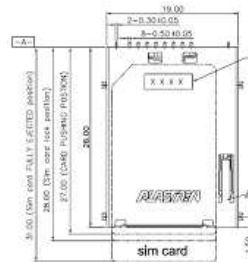
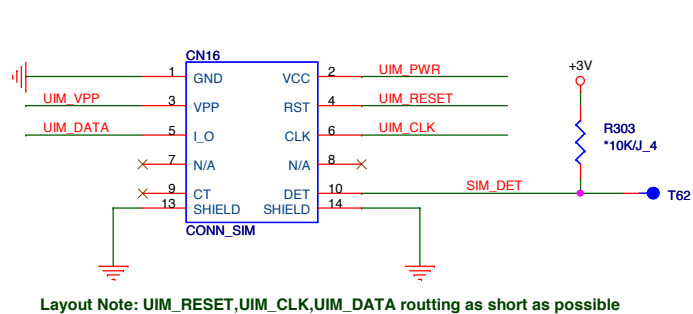


EC-A-06: Remove AOAC SCH because AMD can not support AOAC.

EC-B-09: Add AOAC SCH back because Lenovo request.



## SIM Card CONN



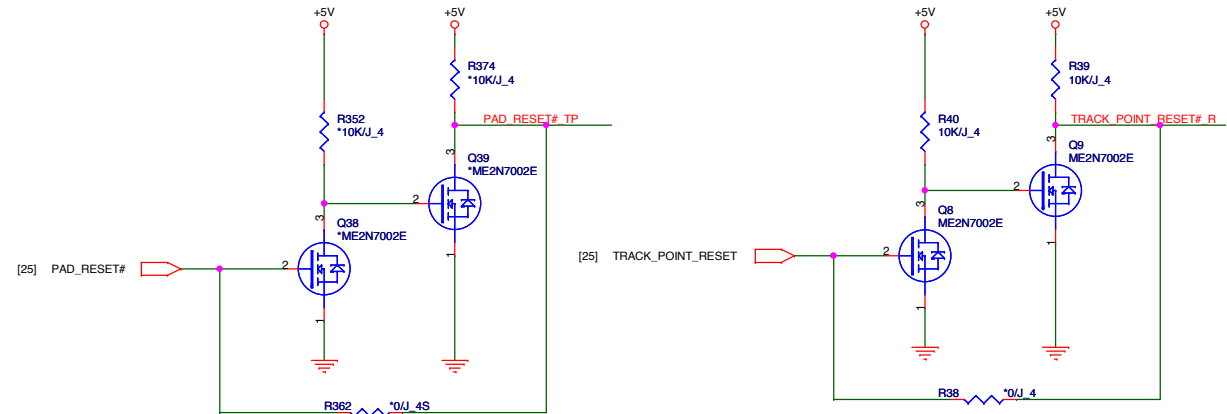
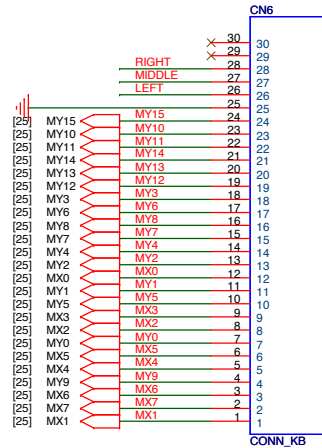
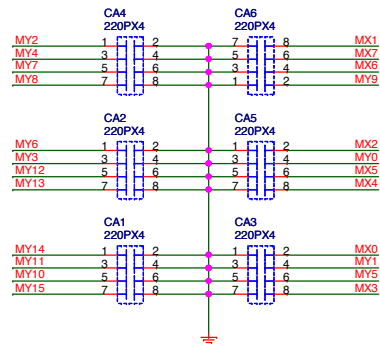
Quanta Computer Inc.

PROJECT : LI2A

Size	Document Number	Rev
	CONN WWAN or mSATA	3A

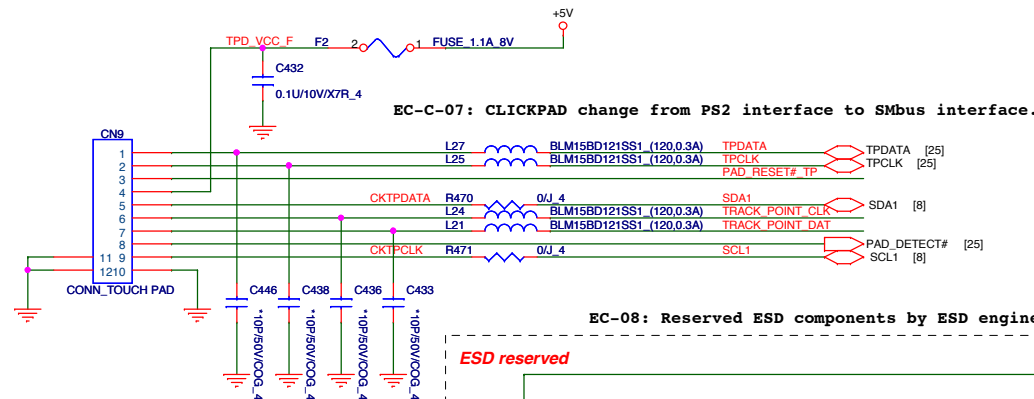
Date: Monday, April 09, 2012 Sheet 18 of 40

For EMI request



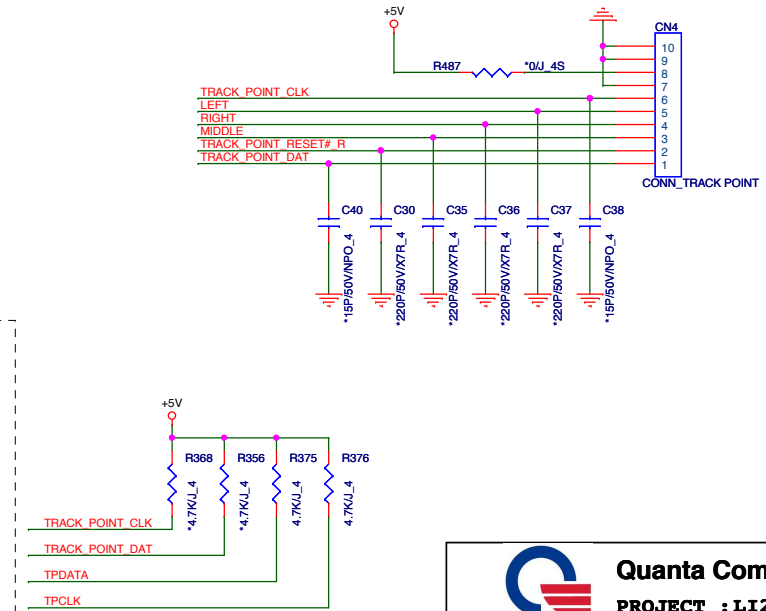
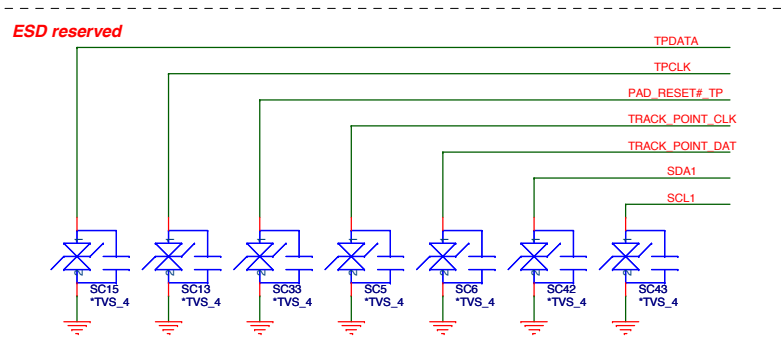
## TOUCH PAD

## TRACK POINT



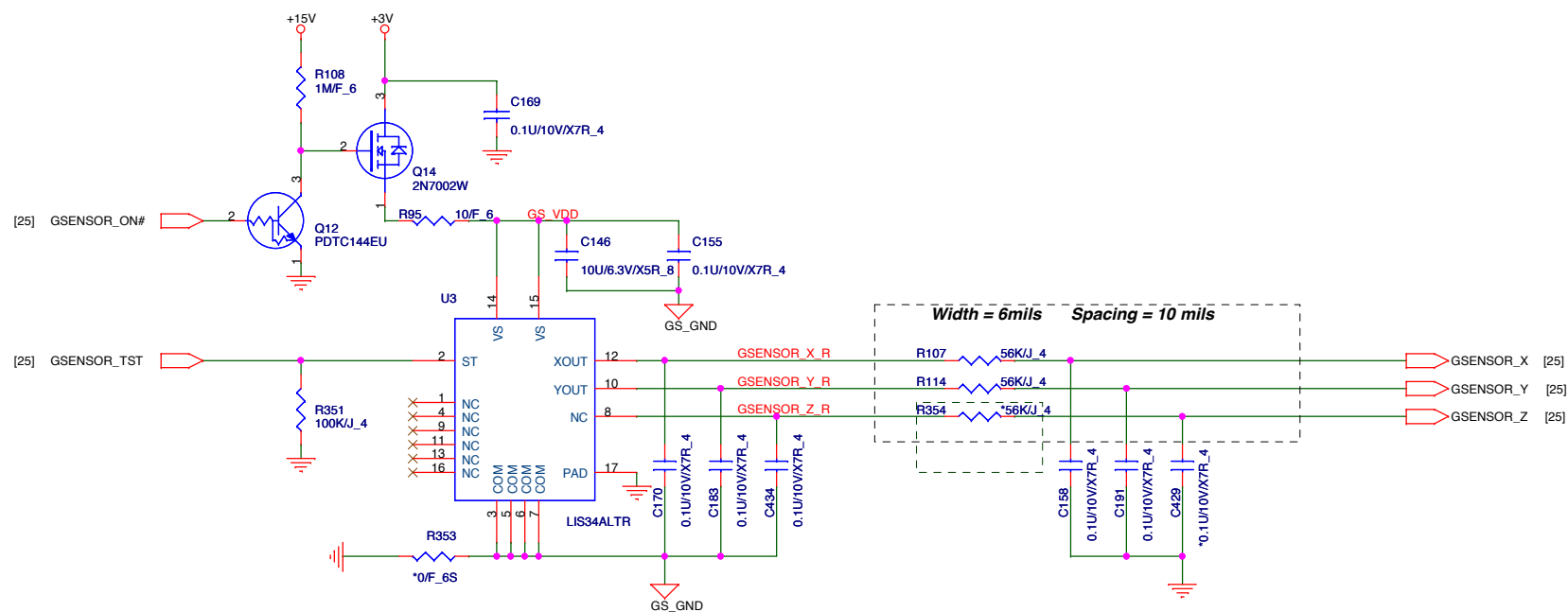
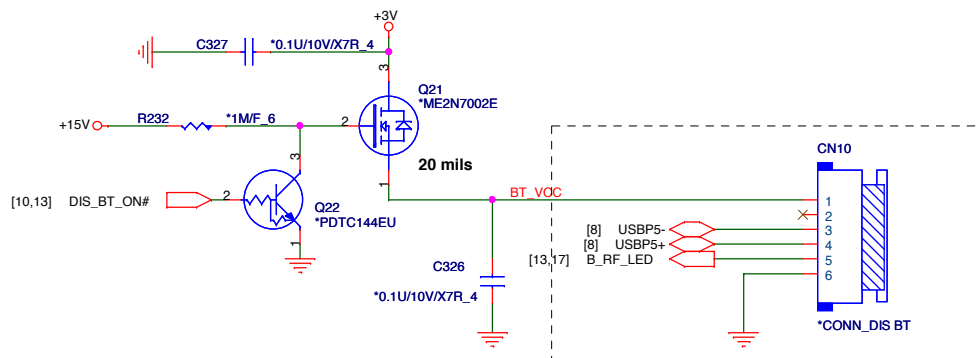
EC-B-10: Reverse Smbus CLICKPAD SCH.

EC-08: Reserved ESD components by ESD engineer's suggestions



## G-SENSOR (2-Axial)

## EC-25: Change Pin Define



The schematic diagram illustrates the LANVCC power supply circuit. It features a 3V<sub>PCU</sub> input connected to a diode (D20, AOS402A) and a resistor (R221, 0Ω<sub>BS</sub>). The diode's cathode is connected to the LANVCC node, which is also connected to a resistor (R221, 0Ω<sub>BS</sub>). The diode's anode is connected to the LANVON signal (pin 3 of a connector) and a resistor (R221, 0Ω<sub>BS</sub>). The LANVCC node is connected to a capacitor (C310, 100nF/3V/XSR\_8) and a resistor (R221, 0Ω<sub>BS</sub>). The LANVCC node is also connected to a resistor (R221, 0Ω<sub>BS</sub>) and a capacitor (C298, 0.1uF/10V/X7R\_4).

**LANVCC**  
Trace width>60mil,  
Trace length<200mil

LAN\_EVDD12

**Place CAP. close to LAN IC pin 3,6,9,13,29,41,45**

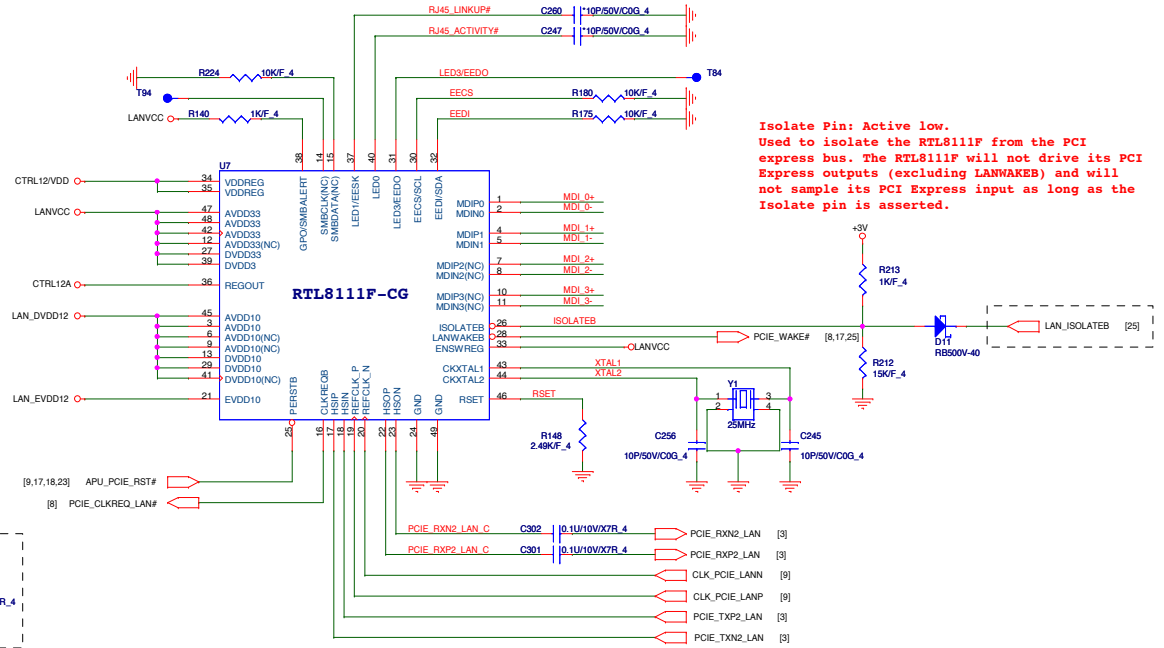
**Place CAP. close to LAN IC pin 34, 35**

**Layout:**All termination signal should have 20 mil trace

[illegible]

EC-A-09: Add 1M ohm (1206) & reserve 1M ohm (0603) to pass Hi-Pot & ESD test.

Reserve for Surge and cable ESD



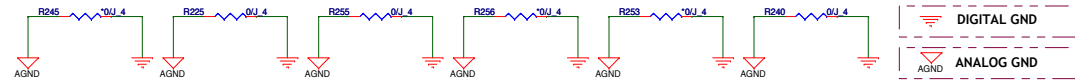
Isolate Pin: Active low.  
Used to isolate the RTL811F from the PCI express bus. The RTL811F will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

The diagram illustrates the LAN interface circuit. It features two RJ45 ports, RJ45\_1 and RJ45\_2, each with a 100Ω termination resistor (R380, R390, R414) connected to LAN\_VCC. The ports are connected to a LAN controller (LANC) via a connector (CN27). The LAN controller has pins for LAN\_LED, LAN\_RX, LAN\_TX, LAN\_RXD, LAN\_TXD, LAN\_RX+, LAN\_TX+, LAN\_RX-, LAN\_TX-, LAN\_RXAcTIVITY#, and LAN\_GND. The LAN controller is connected to a LAN controller chip (LANC) via a connector (CN27). The LAN controller chip has pins for LAN\_LED, LAN\_RX, LAN\_TX, LAN\_RXD, LAN\_TXD, LAN\_RX+, LAN\_TX+, LAN\_RX-, LAN\_TX-, LAN\_RXAcTIVITY#, and LAN\_GND. The LAN controller chip is connected to a LAN controller chip (LANC) via a connector (CN27). The LAN controller chip has pins for LAN\_LED, LAN\_RX, LAN\_TX, LAN\_RXD, LAN\_TXD, LAN\_RX+, LAN\_TX+, LAN\_RX-, LAN\_TX-, LAN\_RXAcTIVITY#, and LAN\_GND. The LAN controller chip is connected to a LAN controller chip (LANC) via a connector (CN27). The LAN controller chip has pins for LAN\_LED, LAN\_RX, LAN\_TX, LAN\_RXD, LAN\_TXD, LAN\_RX+, LAN\_TX+, LAN\_RX-, LAN\_TX-, LAN\_RXAcTIVITY#, and LAN\_GND.

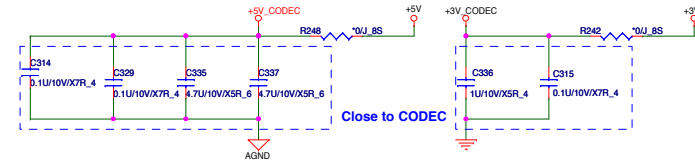
**AUDIO CODEC: ALC3202-VC3-GR**

**EMI Reserve**

**Please see Design Guide for audio grounding.**

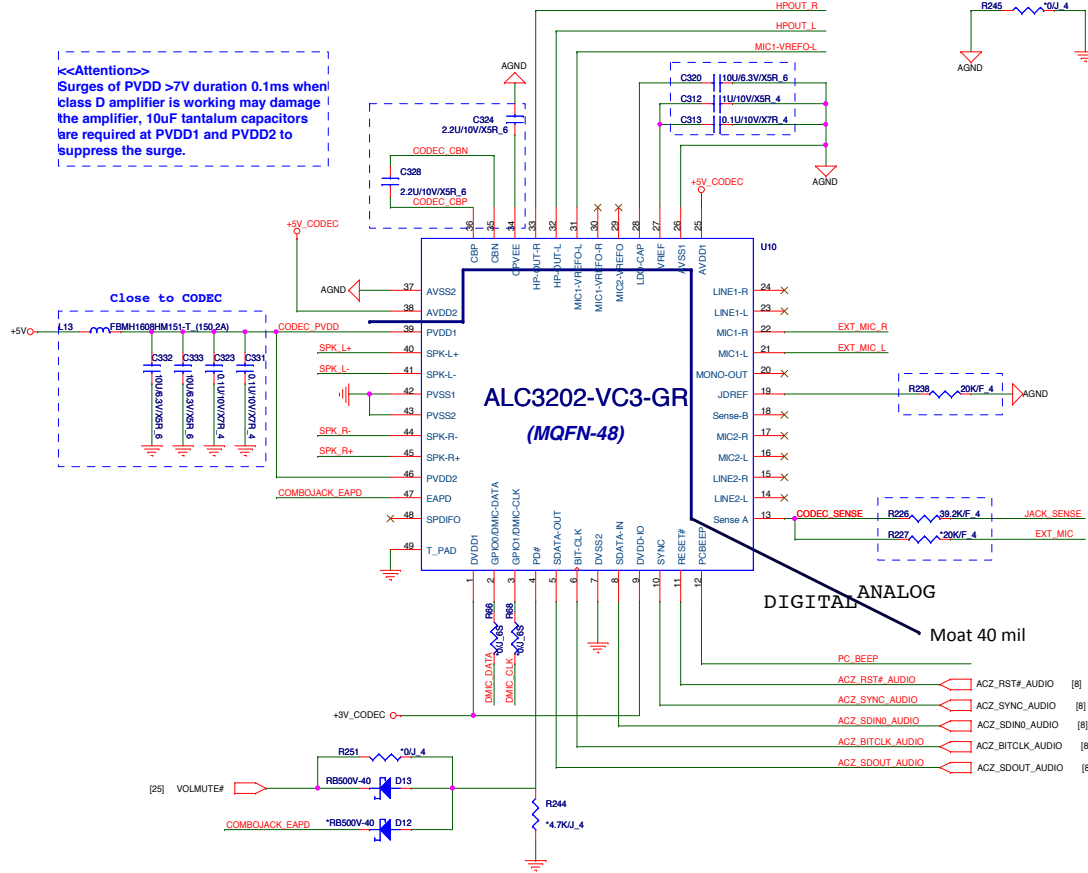
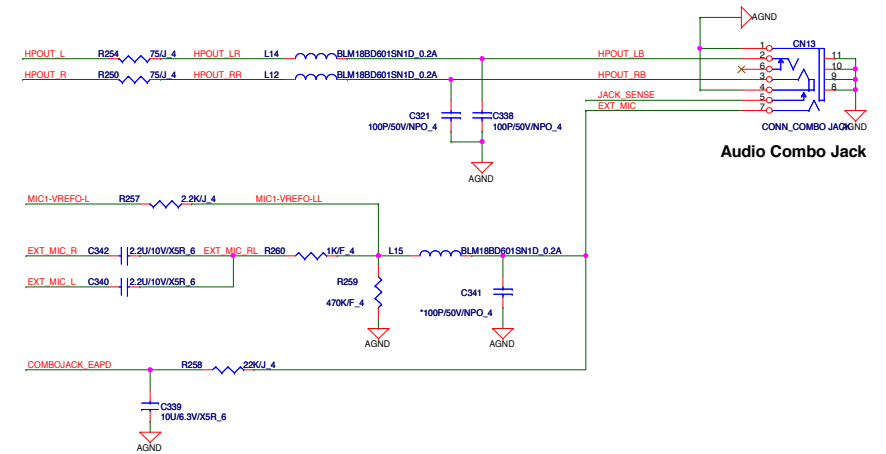


**POWER**

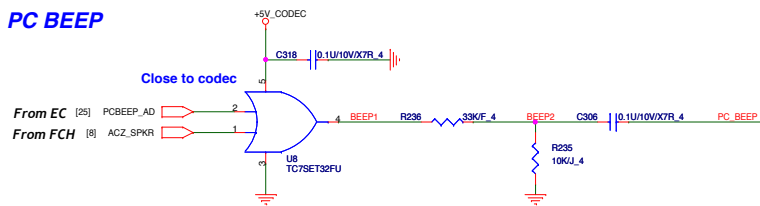


### External MIC/Headphone Combo

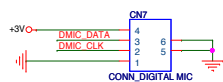
**Important for Jack detect behavior: The Pin 4 & Pin 5 of COMBO-JACK must use Normal-Open type.**



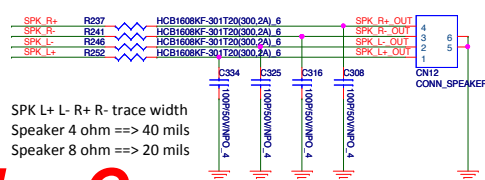
**PC BEEP**



**INT Digital MIC**

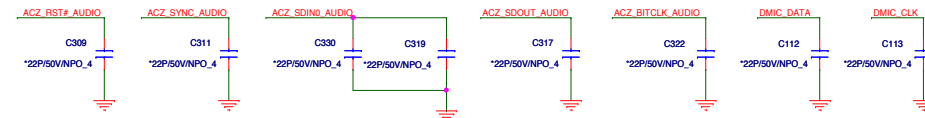


**INT Speaker**

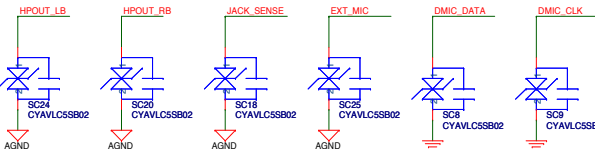


**EMI Reserve**

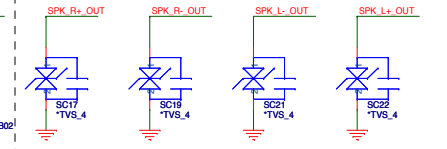
**Place there EMI components next to codec; For EMI issue, please also refer our ALC269 Layout guide document**

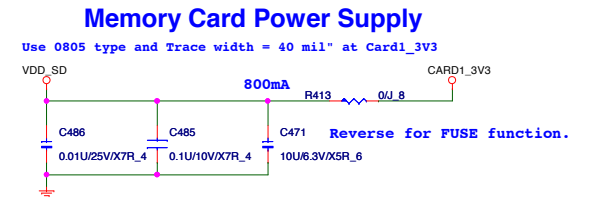
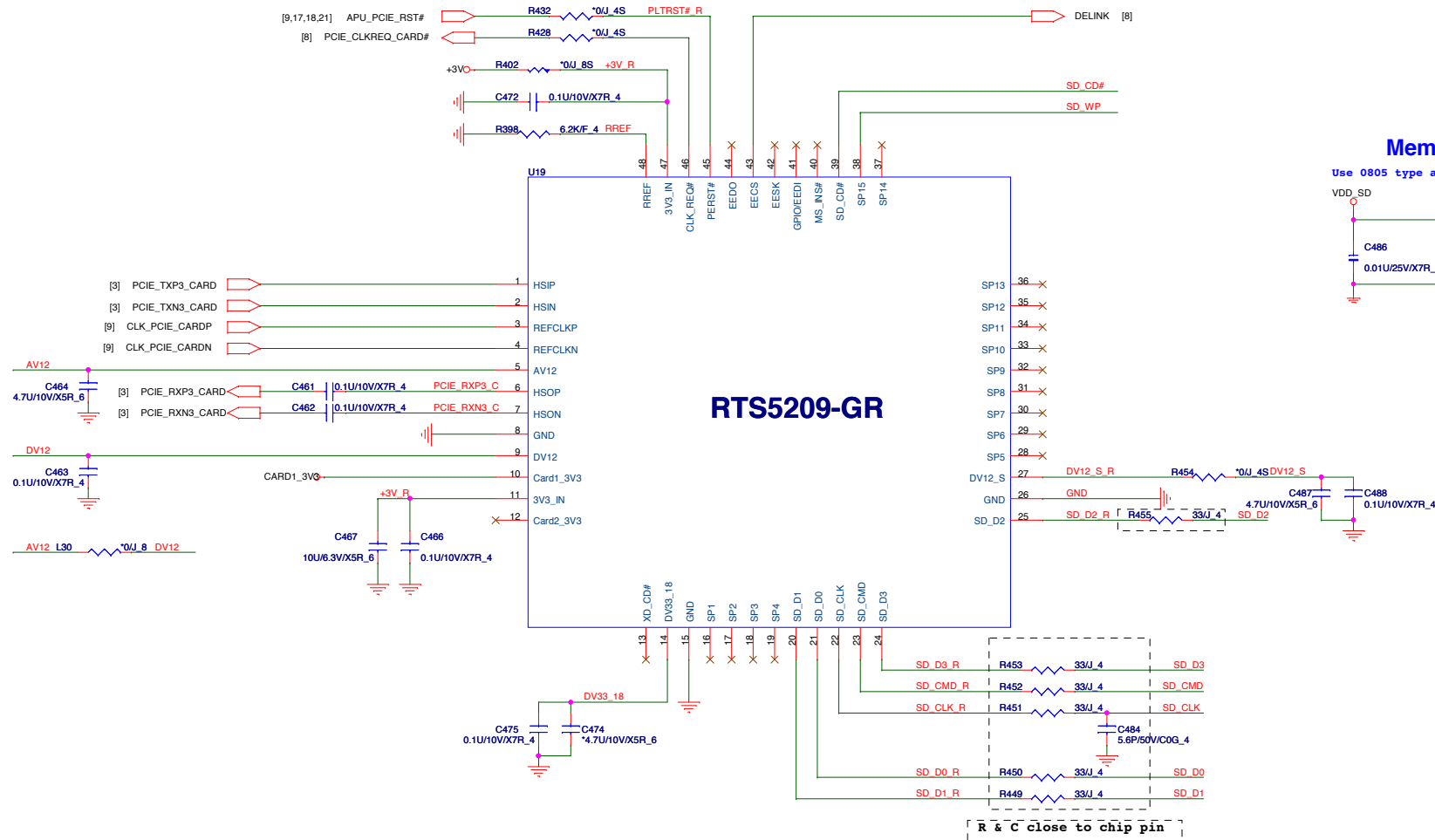


**ESD Reserve**

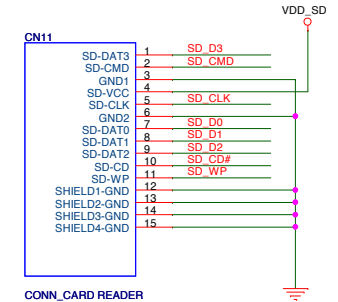


EC-08: Reserved ESD components by ESD engineer's suggestions



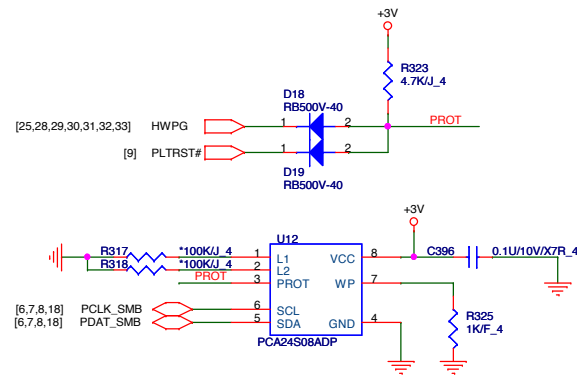


## 4 IN 1 CARD READER SD/SDHC/SDXC/MMC



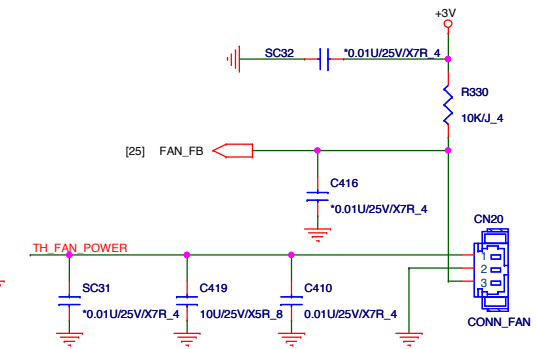
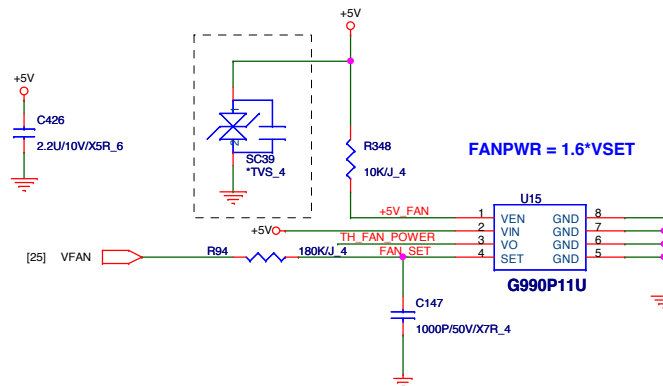
It is recommended that mismatch trace length between CLK and DATA trace is 100 mils with maximum  
EC-A-18: Add 33 ohm in card reader related SCH to match vendor suggestions & EMI test.

## RFID



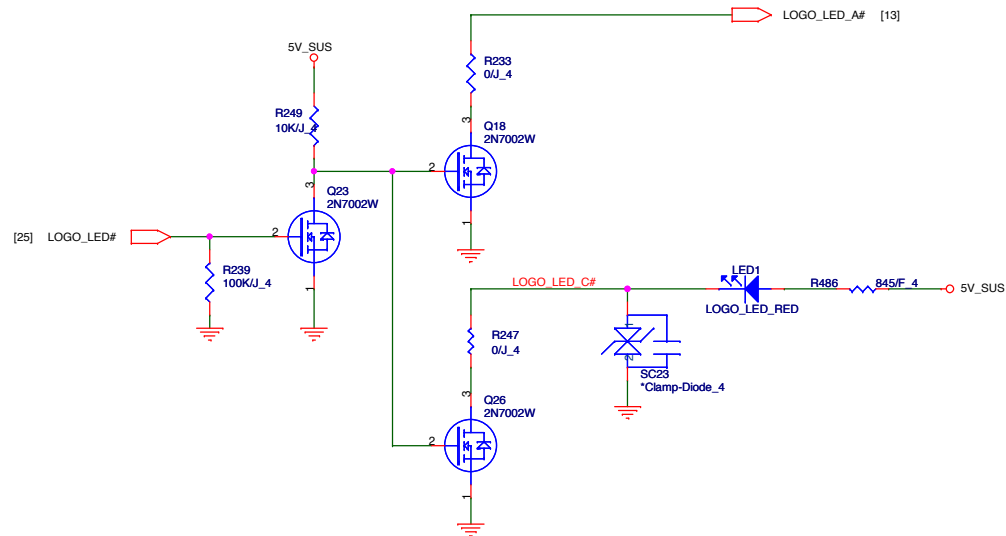
## FAN IC &amp; CONN

EC-B-15: Reverse ESD solutions for USB3.0.

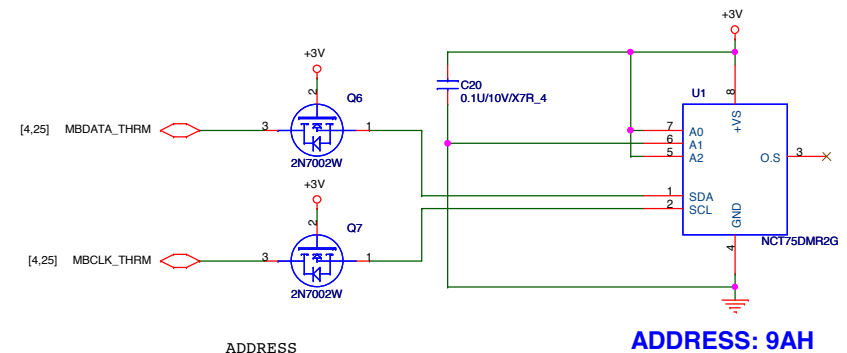


EC-17: Reserved ESD components by ESD engineer's suggestions

## LED Driver

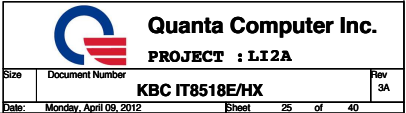


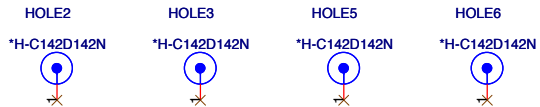
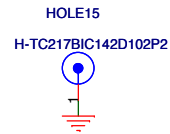
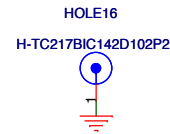
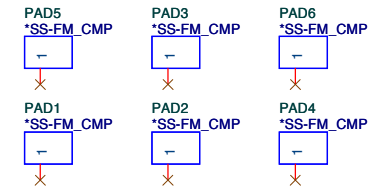
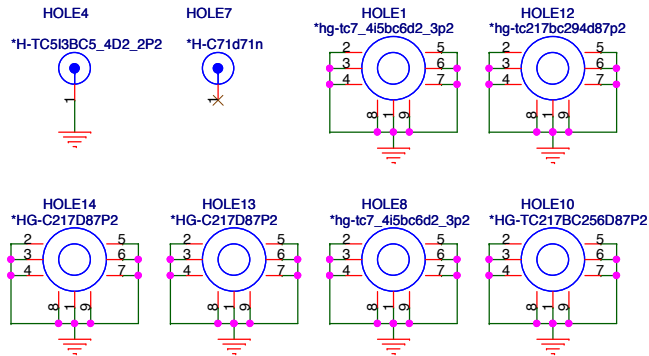
## Thermal IC for Charger



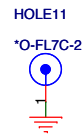
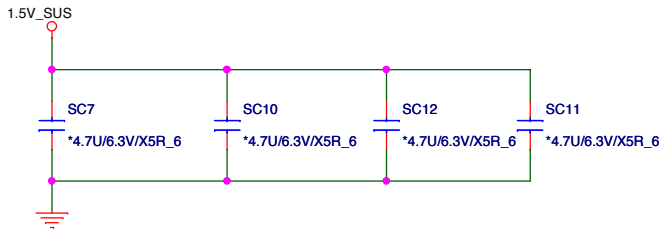
ADDRESS: 9AH





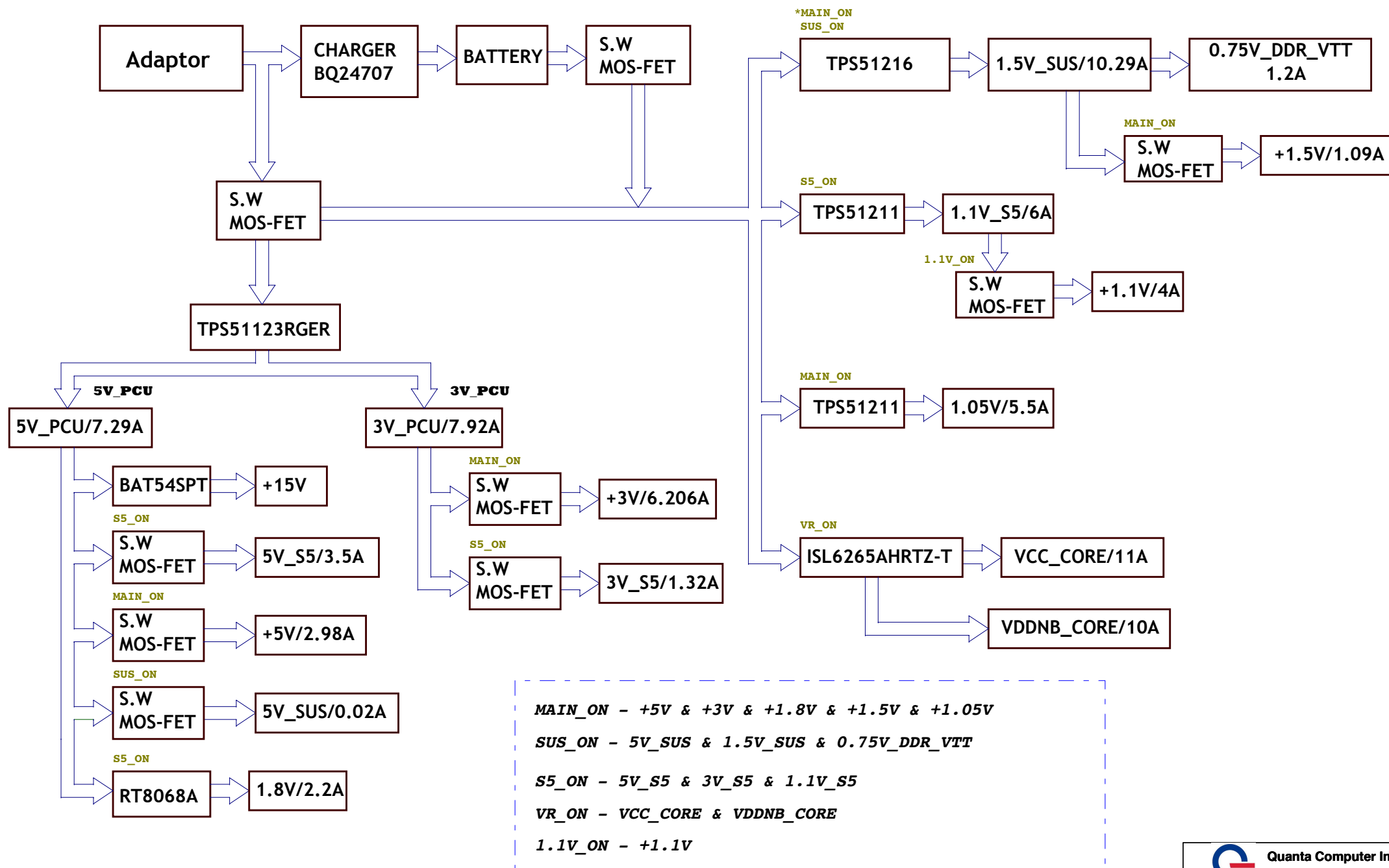
**Hole For CPU support****MiniCard WWAN****MiniCard WLAN****Optics Point****Boundary Hole****CRT PAD**

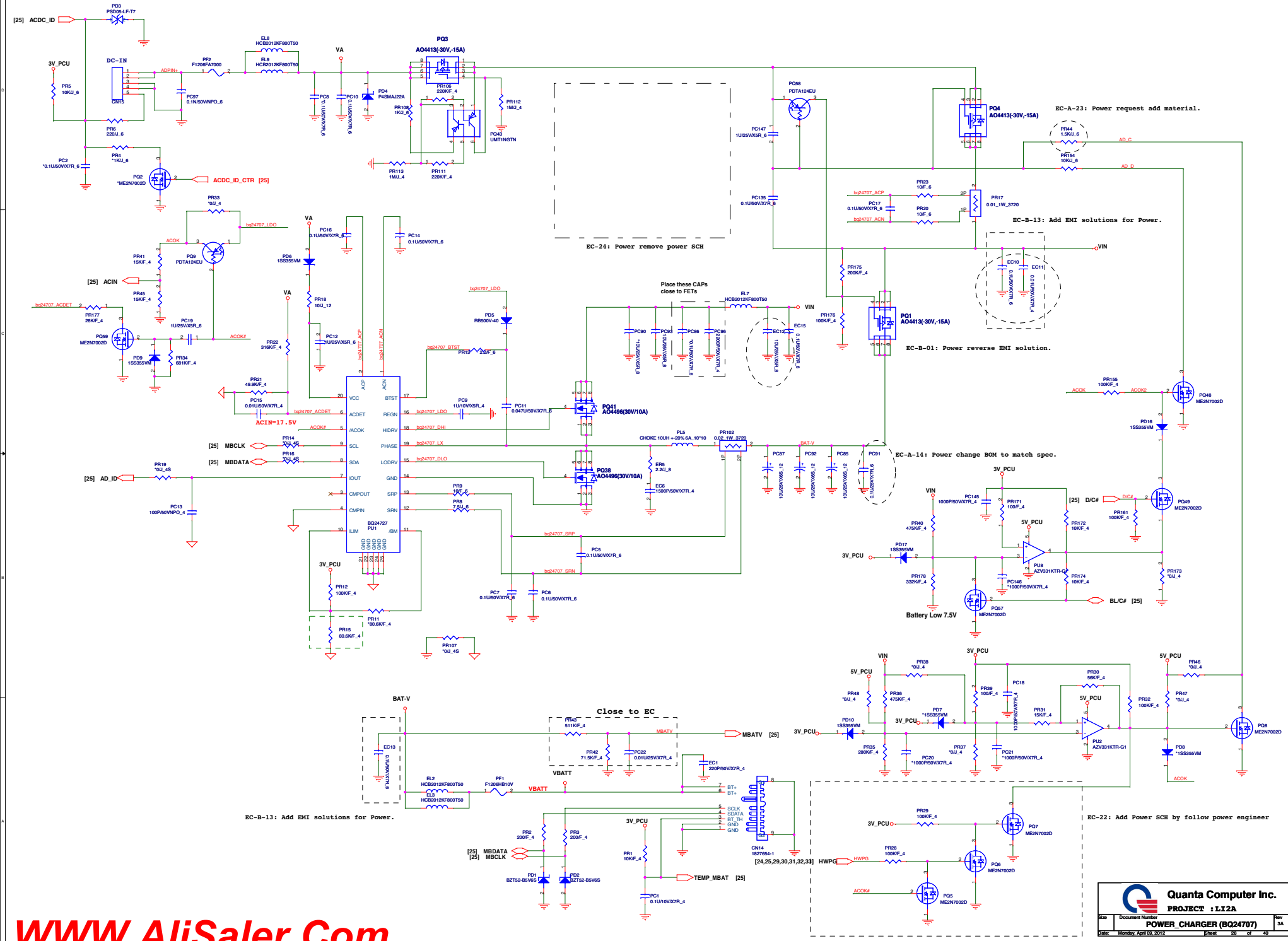
HOLE9

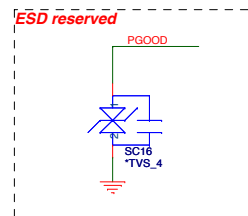
**Keyboard****EC-15: Reserved ESD components by ESD engineer's suggestions****Quanta Computer Inc.****PROJECT : LI2A**

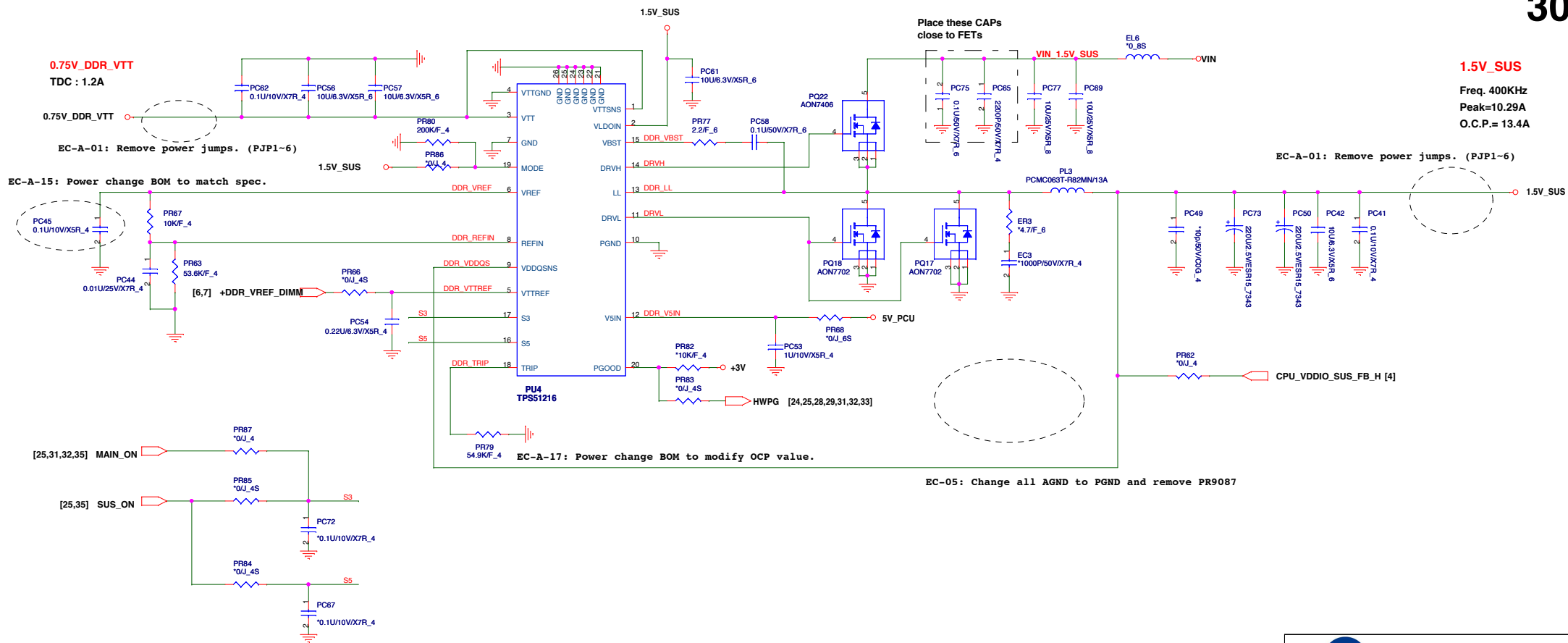
Size	Document Number	Rev
	<b>Screw Hole/EMI/ESD</b>	3A
Date:	Thursday, March 29, 2012	Sheet 26 of 40

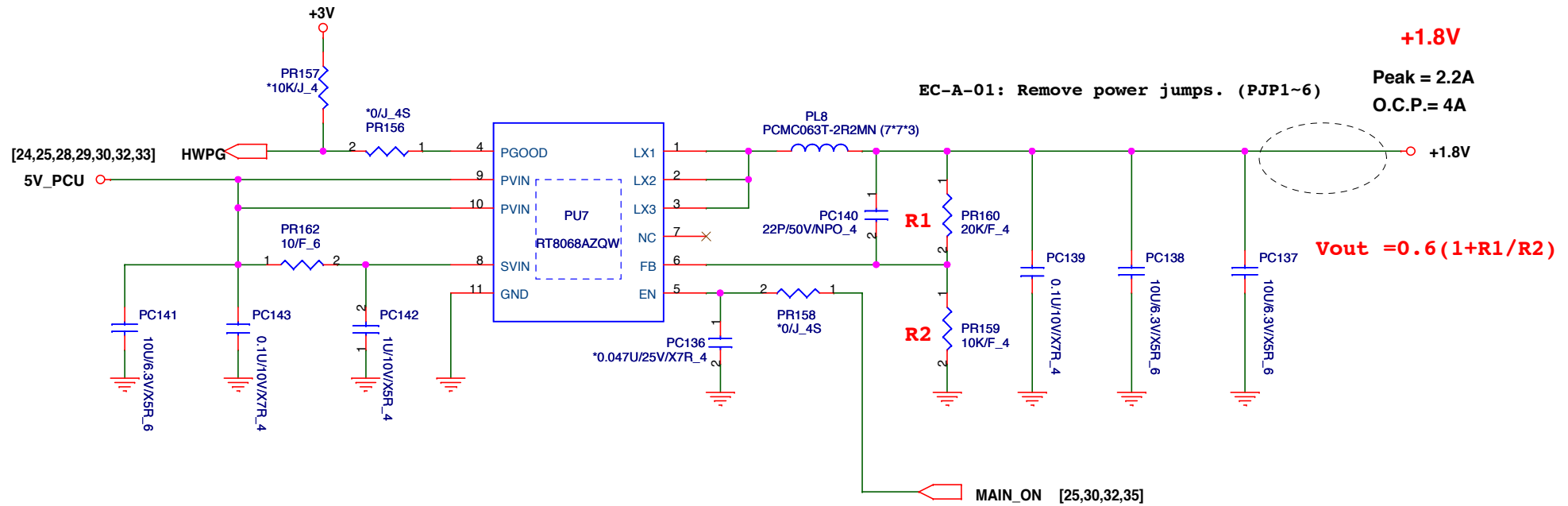
# AMD BRAZOS 2.0 SYSTEM POWER BLOCK DIAGRAM









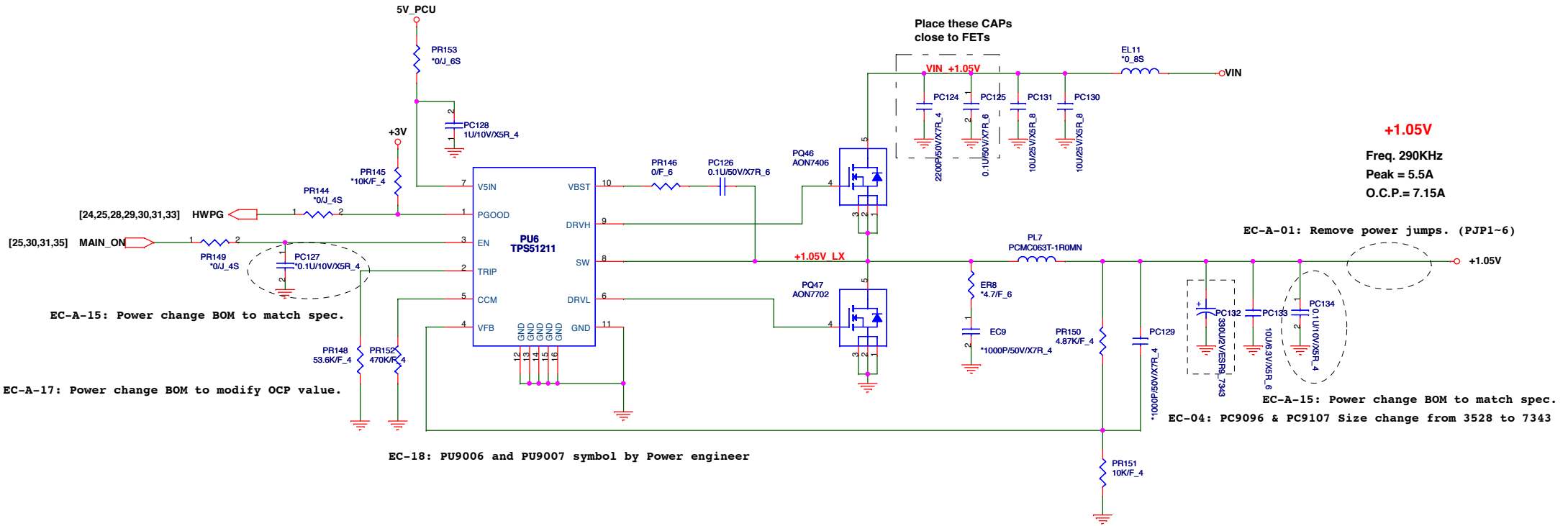



Quanta Computer Inc.

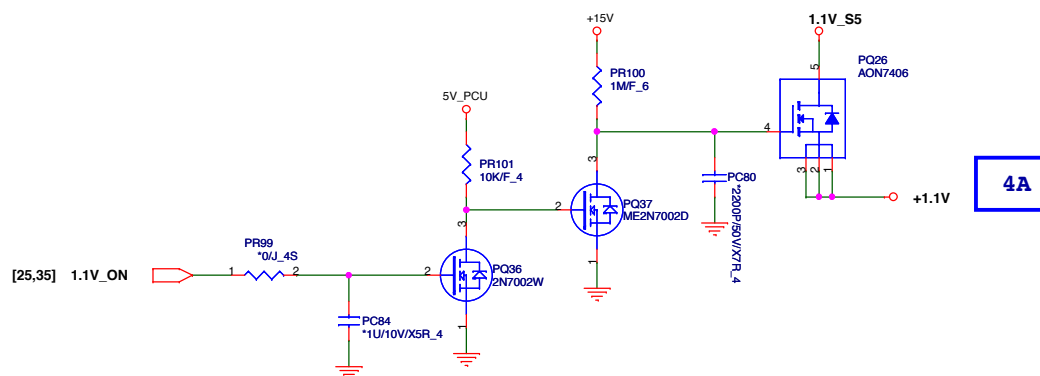
PROJECT : LI2A

Size	Document Number	Rev
	<b>POWER_+1.8V (RT8068)</b>	3A

Date: Monday, April 09, 2012 Sheet 31 of 40

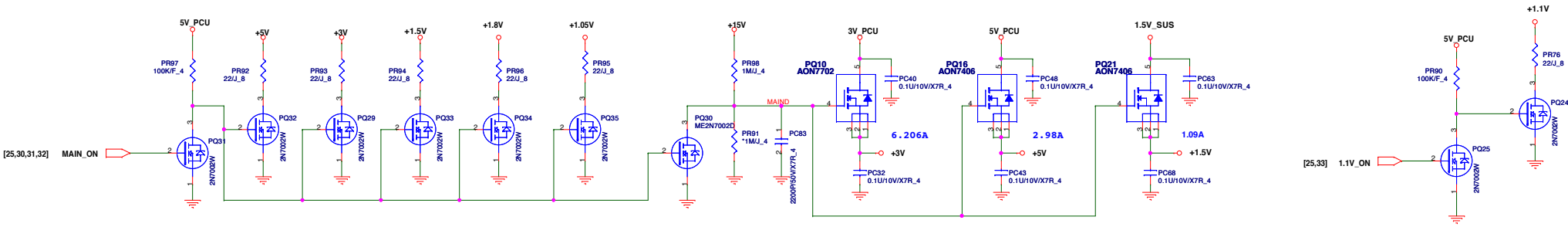


 <b>Quanta Computer Inc.</b> <b>PROJECT : LI2A</b>		
Size	Document Number	Rev
	<b>POWER_+1.05V (TPS51211)</b>	3A
Date	Monday, April 09, 2012	Sheet 32 of 40



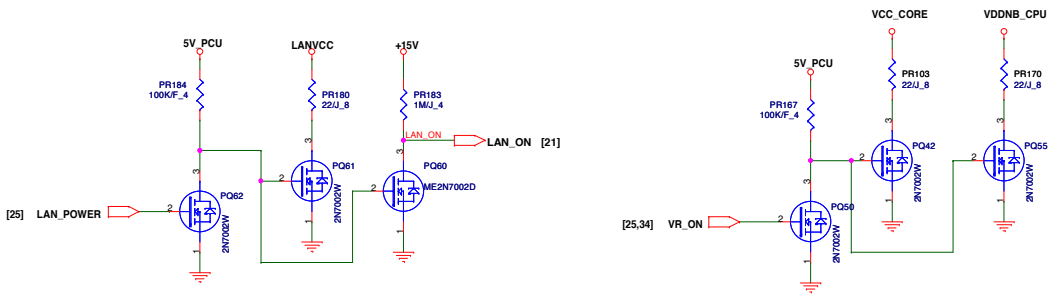


+3V, +5V, +1.8V, +1.5V, 1.05V



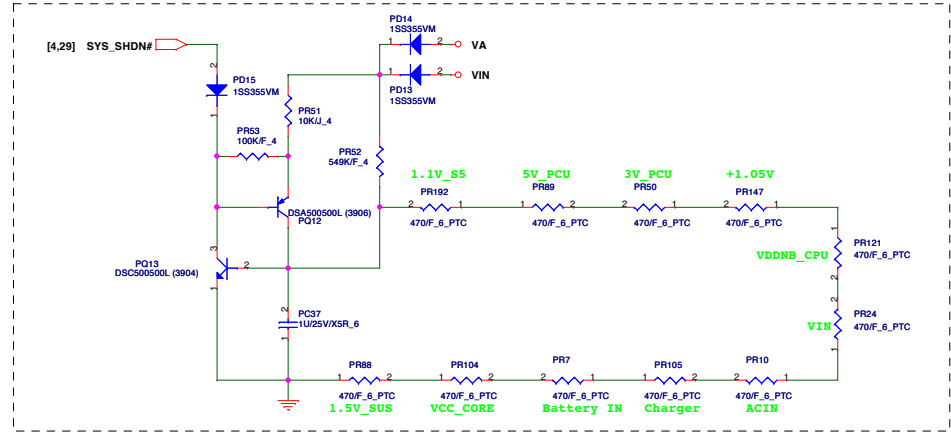
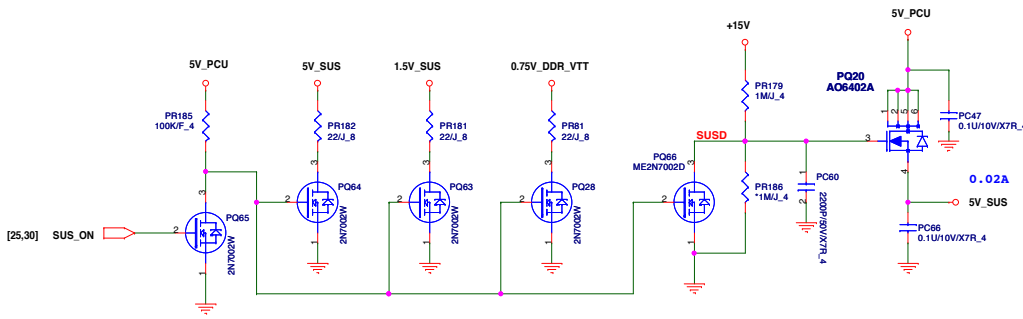
LANVCC

VCC\_CORE, VDDNB\_CPU



EC-11: Modify PTC NAME: PR9178(1.1V\_S5), PR9179(5V\_PCU), PR9180(3V\_PCU)PR9181(+1.05V), PR9184(VDD\_NBCPU), PR9189(VIN), PR9194(ACIN), PR9193(CHARHER), PR9192(Battery IN), PR9191(VCC\_CORE), PR9196(1.5V\_SUS).

5V\_SUS, 1.5V\_SUS, 0.75V\_DDR\_VTT



## Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release		

## Schematic Value Explanation Description :

### RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005 )					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K/J_6	5%		0603 (1608 )				POP	1K ohm 5% SMD 0603 package and POP
1K/J_8	5%			0805 (2125 )			POP	1K ohm 5% SMD 0805 package and POP
1K/J_12	5%				1206 (3216 )		POP	1K ohm 5% SMD 1206 package and POP
1K/J_1210	5%					1210 (3225 )	POP	1K ohm 5% SMD 1210 package and POP

### CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005 )				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608 )				POP	0.1UF 25V X7R SMD 0603 package POP

# LI2A-AMD Schematic EC Tracking Record (Before A stage) 2011.11.10

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EC-01: Remove SATA redriver & other components

EC-02: Remove AMD HDMI related components

EC-03: CCD power changes from +5V to +3V

EC-04: PC9096 & PC9107 Size change from 3528 to 7343

EC-05: Change all AGND to PGND and remove PR9087

EC-06: Reserved ESD components by ESD engineer's suggestions

EC-07: Add ESD components by ESD engineer's suggestions

EC-08: Reserved ESD components by ESD engineer's suggestions

EC-09: Reserved ESD components by ESD engineer's suggestions

EC-10: Reserved ESD components by ESD engineer's suggestions

EC-11: Modify PTC NAME: PR9178(1.1V\_S5), PR9179(5V\_PCU),  
PR9180(3V\_PCU)PR9181(+1.05V), PR9184(VDD\_NBCPU),  
PR9189(VIN), PR9194(ACIN), PR9193(CHARHER),  
PR9192(Battery IN), PR9191(VCC\_CORE), PR9196(1.5V\_SUS).

EC-12: Page29 pin14 add PR and net 5V\_AL

EC-13: Reserved ESD components by ESD engineer's suggestions

EC-14: Change EMI sloution by follow PT-Note

EC-15: Reserved ESD components by ESD engineer's suggestions

EC-16: Reserved ESD components by ESD engineer's suggestions

EC-17: Reserved ESD components by ESD engineer's suggestions

EC-18: PU9006 and PU9007 symbol by Power engineer

EC-19: Hall IC power changes from 3V\_S5 to 3V\_PCU

EC-20: Add HDMI level shifter second source BOM control table

EC-21: Add mSATA GPIO pin pull up

EC-22: Add Power SCH by follow power engineer

EC-23: add WWAN, WLAN, BT LED SCH to match Jett spec

EC-24: Power remove power SCH

EC-25: Change Pin Define

# LI2A-AMD Schematic EC Tracking Record (After A stage) 2011.12.19

38

EC-A-01: Remove power jumps. (PJP1~6)

EC-A-02: EC engineer requested KBSMI# & SCI# must pull up to +3V by 10K.  
Add CS31002JB28 - R456 & R457

EC-A-03: Modify CCD power source width.  
Add: CS00003J951 - R458  
Remove: CS00002JB38 - R11 & \*R12

EC-A-04: EE implement HW Board ID to decide Dutton or Jett & APU.  
Add: CS31002JB28 - R381 & R369  
Remove: CS31002JB28 - R383 & R371

EC-A-05: Add diode for HDMI power  
Add: BCRB500VZ29 - D20

EC-A-06: Remove AOAC SCH because AMD can not support AOAC.  
Remove: CS00002JB38 - R167

EC-A-07: Add Fuse to meet DV test.  
Add: DK300WFU203 - F3  
Remove: CS00003J951 - R10

EC-A-08: Add 0 ohm to CCD power.  
Add: CS00003J951 - R459

EC-A-09: Add 1M ohm (0603) & reserve 1M ohm (1206) to pass Hi-Pot & ESD test.  
Add: CS51003F934 - R460  
Remove: CS51003F934 - R231

EC-A-10: Add 10K ohm to pull up HWPG  
Add: CS31002JB28 - R462

EC-A-11: Change PN for power sequence.  
Add: BCBAT54AZ02 - D10  
Remove: BCBAT54CZ04 - D10

EC-A-12: Modify ROM SCH to add Power.

EC-A-13: Modify BOM to match SCH.  
Remove: CS00002JB38 - R155

EC-A-14: Power change BOM to match spec.  
Change: From CH41006K911 to CH41004K910 - PC91 & PC144

EC-A-15: Power change BOM to match spec.  
Change: From CH4104K9B03 to CH41002KB93 - PC45, \*PC127, PC134, \*PC152, PC158

EC-A-16: Power change BOM to match spec.  
Add: CS-4703J917 - ER6 & ER7  
CH21006JB10 - EC7 & EC8

EC-A-17: Power change BOM to modify OCP value.  
Change:  
From CS41402FB14 to CS41102FB13 - PR57  
From CS41202FB17 to CS41102FB13 - PR73  
From CS36802FB00 to CS35492FB14 - PR79  
From CS37502FB12 to CS35362FB17 - PR148  
From CS25902FB10 to CS25492FB12 - PR193  
From CS38062FB14 to CS35492FB14 - PR190  
From CS26492FB23 to CS25112FB15 - PR114  
From CS39762FB12 to CS41002FB28 - PR128  
From CS31962FB18 to CS31692FB11 - PR134

EC-A-18: Add 33 ohm in card reader related SCH to match vendor suggestions & EMI test.  
Add: CH-5606TB01 - C484  
Change: from CS00002JB38 to CS03302JB29 - R449, R450, R451, R452, R453, R455.


EC-A-19: Lenovo modify LED brightness.  
Change:  
from CS21002FB24 to CS11202FB11 - R1.  
from CS21002FB24 to CS11502FB21 - R4.

EC-A-20: AMD Check list error. This change made HDMI Function OK.  
Add: CS21002FB24 - R33.  
Remove: CS21002FB24 - R30.

EC-A-21: ESD request.  
Add: BCC00202Z00 - SU1

EC-A-22: EE request in order LED action error by DIS\_BT  
Remove: BAM70020004 - Q25.

EC-A-23: Power request add material.  
Add: CS21503J947 - PR44.

		Quanta Computer Inc.	
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# LI2A-AMD Schematic EC Tracking Record (After B stage) 2012.2.11

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EC-B-01: Power reverse EMI solution.

Add: CH41006K911 - EC10  
CH31006KB18 - EC11

EC-B-02: Power cost to delete 0 ohm.

Remove:  
CS00002JB38 - PR14,PR16,PR19,PR55,PR64,PR72,PR74,PR66,PR83,PR84,PR85,PR156,PR158,PR144,PR149,  
PR99,PR187,PR191,PR115,PR118,PR119,PR130,PR131,PR132,PR138,PR139,PR141  
CS00003J951 - PR56,PR61,PR68,PR153,PR195

EC-B-03: In order to pass EA clock and meet clock spec.

Add: CH-4706TB01 - C489,C490,C491,C492,C493,C494

EC-B-04: Remove R344 in order to close combo BT.

Remove: CS31002JB28 - R344

EC-B-05: Modify BIOS ROM SCH.

EC-B-06: Modify HDMI detect pin by AMD confirm.

Remove: CS41002JB20 - R270  
CS31002JB28 - R285  
BAM700200F6 - Q31

EC-B-07: Modify BOM to match HDMI Vendor suggestion. BOM table changed.

EC-B-08: Modify Xtal BOM.

Change : C459,C465 from CH0156K0B06 to CH01806JB07

EC-B-09: Add AOAC SCH back because Lenovo request. Reverse AOAC & pcie\_wake to EC.

EC-B-10: Reverse SMBus CLICKPAD SCH.

Add: CS00002JB38 - R472,R473

EC-B-11: Add ESD solutions for HDMI.

Add: BC00511PZ00 - SC34  
CY4025R0B00 - SC35  
CH4102K1B03 - SC36  
CY000390B01 - SC37  
CYAVLC15B00 - SC38

EC-B-12: Add ESD solutions for LAN.

Add: CH4102K1B03 - C495  
Change: C296 change from CH31004KB17 to CH4102K1B03

EC-B-13: Add EMI solutions for Power.

Add: CX000800506 - EL1  
CH41006K911 - EC13,EC14  
CH6104K9A00 - EC12  
CH41006K911 - EC15  
Remove: CH6104K9A00 - PC90  
CH41006K911 - PC86  
Change: PR13 change from CS00003J951 to CS-2203F911  
ER5 change from CS-4703J917 to CS-2204JA37  
EC6 change from CH21006JB10 to CH21506KB14

EC-B-14: Reverse HW shutdown SCH.

EC-B-15: Reverse ESD solutions for USB3.0.

Change: SU2,SU3 change from BCDF1004Z00 to AL000524U02

EC-B-16: Delete DIS\_BT SCH.

Remove: CS00002JB38 - R379  
CS51003F934 - R234,R232  
CH4102K1B03 - C327  
BAM700200F6 - Q19,Q21  
BA001440Z87 - Q22,Q24  
DFHD06MR590 - CN10

EC-B-16: Delete EE 0 ohm in order to cost down.


Remove:  
CS00002JB38 - R296,R297,R298,R299,R300,R301,R302,R304,R273,R286,R26,R70,R109,  
R206,R418,R401,R417,R336,R349,R14,R41,R365,R117,R139,R146,R177,R176,R132,R112,  
R113,R129,R128,R432,R428  
CS00003J951 - R27,R28,R43,R46,R47,R99,R104,R98,R433,R115  
CS00004JA40 - R161,R386,R364,R186,R120,R261,R308,R319,R221,R222,R228,R248,  
R242,R413  
CS00003F916 - R353

EC-B-17: Reverse R477 FOR ICT TEST.

EC-B-18: Reverse mSATA & WWAN detect pin SCH to EC.

EC-B-19: ESD modify SCH & PN to pass ESD test.

Add: CYAVL5M0B00 - C499,C501  
BC101304Z00 - SU7,SU8

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# LI2A-AMD Schematic EC Tracking Record (After C stage) 2012.2.11

39

EC-C-01: Drop CCD Led relation BOM.

Remove: BAM70020004 - Q2

CS11502FB21 - R4

EC-C-02: Change RF Led power from +3V to +5V.

Change: R1 change from CS11202FB11 to CS00002JB38

Add: R483,R484 - CS11203F918

Reserve: SC41

EC-C-03: Reserve HDD LED

Reserve: R481,LED2,SC40

EC-C-04: Change HDMI SCH from diode to load switch.

Remove: BCRB500VZ29 - D20

DK110TPU006 - F1

Add: AL002331000 - U21

CH4102K1B03 - C503,C504

EC-C-05: Change LED SHORT PROTECT.

Add:

CS18452FB11 - R486

CS21802FB10 - R482

Change:

R233 from CS21802FB10 to CS00002JB38

R247 from CS18452FB11 to CS00002JB38

EC-C-06: Modify mSATA detect SCH.

Add: CS00002JB38 - R479

Remove: CS00002JB38 - R74

CS31002JB28 - R79

Reserve: CS31002JB28 - R485

EC-C-07: CLICKPAD change from PS2 interface to SMBus interface.

Add: CS00002JB38 - R470,R471

Remove: CS00002JB38 - R472,R473

EC-C-08: Remove RTC shortpad.

EC-C-09: Delete EE 0 ohm in order to cost down.

Add:

CS00004JA40 - R413

CS00002JB38 - R478

Remove:

CS00002JB38 -

R5,R8,R20,R22,R29,R34,R36,R52,R58,R59,R60,R61,R83,R84,R87,R88,

R89,R90,R101,R102,R103,R122,R123,R130,R165,R166,R168,R172,R188,

R191,R201,R281,R290,R310,R314,R337,R342,R362,R366,R367,R408,R447,

R454,R472,R473

CS00003J951 - R66,R68,R145,R211,R214,R458

CS00004JA40 - R97,R220,R402

EC-C-10: Remove CML1 & R5 & R8 in order to place R483 & R484

		<b>Quanta Computer Inc.</b>	
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